File   9:Business & Industry(R) Jul/1994-2004/Jan 07
         (c) 2004 Resp. DB Svcs.
File 16:Gale Group PROMT(R) 1990-2004/Jan 08
         (c) 2004 The Gale Group
File 47:Gale Group Magazine DB(TM) 1959-2004/Dec 31
         (c) 2004 The Gale group
File 148:Gale Group Trade & Industry DB 1976-2004/Jan 08
         (c)2004 The Gale Group
File 160:Gale Group PROMT(R) 1972-1989
         (c) 1999 The Gale Group
File 275:Gale Group Computer DB(TM) 1983-2004/Jan 08
         (c) 2004 The Gale Group
File 621:Gale Group New Prod.Annou.(R) 1985-2004/Jan 08
         (c) 2004 The Gale Group
File 636:Gale Group Newsletter DB(TM) 1987-2004/Jan 08
         (c) 2004 The Gale Group
File 649:Gale Group Newswire ASAP(TM) 2004/Dec 31
         (c) 2004 The Gale Group
? ds

Set   Items   Description
S1   2000895   PAGE OR PAGES
S2   915908   BLOCK? ?
S3   2424756   STORAGE OR MEMORY OR BUFFER? ? OR CACHE? ? OR RAM OR ROM OR
              PROM OR EPROM OR FPROM OR CDROM? ?
S4   20928   EDAC OR ECC OR HAMMING
S5   96321   DEBUG? OR DE()BUG???? ?
S6   12251317   CHECK??? ? OR DETECT??? ? OR DIAGNOS???? ? OR DX OR ANALYZ?
              OR ANALYS? OR ANALYT? OR LOOK??? ? OR EXAMIN? OR SCREEN?
S7   9220641   SCRUTIN? OR REVIEW? OR EVALUAT? OR INSPECT? OR MONITOR? OR
             TEST OR TESTS OR TESTED OR TESTING OR SCAN OR SCANS OR SCANNED
              OR SCANNING
S8   240776   ('NOT' OR WITHOUT)(1W)S6:S7
S9   39837   UNCHECK? OR UNEXAMIN? OR UNSCREEN? OR UNSCRUTIN? OR UNREVI-
             EW? OR UNEVALUAT? OR UNINSPECT? OR UNMONITOR? OR UNSCAN????? ?
              OR UNTEST??? ?
S10   3495   S4:S5(3N)('NOT' OR WITHOUT)
S11   2288051   BYPASS? OR BY()PASS??? ? OR AVOID? OR SKIP???? ? OR IGNOR?
             OR DISREGARD? OR EXCLUD? OR EXCLUSION? OR PASS???()OVER
S12   0   'BY'()PASS??? ?
S13   61665   S11:S12(3N)S4:S7
S14   39384   S1:S2(5N)S3
S15   126   S14(S)(S8:S10 OR S13)
S16   47   S15/1999:2003
S17   79   S15 NOT S16
S18   56   RD (unique items)
? t18/3,k/10,13,16

18/3,K/10   (Item 2 from file: 47)
DIALOG(R)File 47:Gale Group Magazine DB(TM)
(c) 2004 The Gale group. All rts. reserv.

04652322   SUPPLIER NUMBER: 18959041   (USE FORMAT 7 OR 9 FOR FULL TEXT)
Power Debugging. (NuMega Technologies' BoundsChecker 4.0 and Pure Atria's Purify for Windows NT debugging software) (includes related article on BoundsChecker's superiority over Purify) (Software Review)(Evaluation)
Boling, Douglas
PC Magazine, v15, n22, p209(4)
Dec 17, 1996
DOCUMENT TYPE: Evaluation   ISSN: 0888-8507   LANGUAGE: English
RECORD TYPE: Fulltext; Abstract

WORD COUNT: 3539 LINE COUNT: 00276

... API, Purify ensures that a pointer passed to a Windows function points to a valid **block** of **memory** , but it does **not** **check** that the parameters are valid for that call. For example, Purify does not verify that...

18/3,K/13 (Item 5 from file: 47)
DIALOG(R)File 47:Gale Group Magazine DB(TM)

03870737 SUPPLIER NUMBER: 13507992 (USE FORMAT 7 OR 9 FOR FULL TEXT)
DOS 6: the ultimate software bundle. (Software Review) (MS-DOS 6.0 operating system)(includes related articles on each set of utilities, Novell Inc's Novell DOS, tips for getting the most out of DOS, highlights, improvements suggested for next version) (Evaluation)
Prosise, Jeff; Ayre, Rick; Barr, Christopher; Gottesman, Ben Z.; Flanders, Bob; Mendelson, Edward; Simon, Barry
PC Magazine, v12, n7, p108(17)
April 13, 1993
DOCUMENT TYPE: Evaluation ISSN: 0888-8507 LANGUAGE: ENGLISH
RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 10431 LINE COUNT: 00791

... recognized by MemMaker.
Tip 2. Configure EMM386.EXE to provide an extra 24K of upper **memory** **block** (UMB) **RAM** . DOS 6's EMM386.EXE driver typically creates more upper memory than its counterpart in...

...upper memory for unused address space. (DOS 5's EMM386.EXE did not.) It does **not** , however, **scan**0 the region from C000h to C5FFh on most PCs, leaving, potentially, 24K of UMB space...

18/3,K/16 (Item 8 from file: 47)
DIALOG(R)File 47:Gale Group Magazine DB(TM)

03457707 SUPPLIER NUMBER: 08731036 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Letters. (letter to the editor)
Stasio, Vincent P.; Kuchta, Bob
PC Week, v7, n32, p64(1)
August 13, 1990
DOCUMENT TYPE: letter to the editor ISSN: 0740-1604 LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT
WORD COUNT: 571 LINE COUNT: 00044

... on the SIMM module. Two typical types of RAM used are Static Column and Fast **Page** Mode.
Although all types of **RAM** may have the same "total" access time (80 nanoseconds, for example), Fast **Page** Mode **RAM** has published timing specifications that the others do not (to be technical, they are Access...

...is counting on these parameters to be consistent during its access sequence and they are **not** , PARITY **CHECK** 2 or system lockup can occur.
To ensure that installing SIMMs will not have a...
? t18/3,k/33

18/3,K/33 (Item 1 from file: 275)

DIALOG(R)File 275:Gale Group Computer DB(TM)

02207492 SUPPLIER NUMBER: 20964142 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Custom performance monitoring for your Windows NT applications. (Product Support)
Richter, Jeffrey
Microsoft Systems Journal, v13, n8, p17(13)
August, 1998
ISSN: 0889-9932 LANGUAGE: English RECORD TYPE: Fulltext; Abstract
WORD COUNT: 7686 LINE COUNT: 00755

... Obviously, performance monitoring is not free. Somewhere inside your application you need to have a **block** of **memory** that stores current counter data. Periodically, your code must update these values. That means that...

...code is going to be larger and will execute slower, something you always try to **avoid** . If performance **monitoring** affected the system drastically, no one would use it. Certainly the speed of performance monitoring...
? t18/3,k/41-42,50

18/3,K/41 (Item 9 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)

01585124 SUPPLIER NUMBER: 13419026 (USE FORMAT 7 OR 9 FOR FULL TEXT)
The Alpha Demonstration Unit: a high-performance multiprocessor. (prototype computer system) (one of four articles on DEC's Alpha architecture) (includes related article on DEC's Alpha chip team) (Cover Story)
Thacker, Charles P.; Conroy, David G.; Stewart, Lawrence C.
Communications of the ACM, v36, n2, p55(13)
Feb, 1993
DOCUMENT TYPE: Cover Story ISSN: 0001-0782 LANGUAGE: ENGLISH
RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 8188 LINE COUNT: 00625

... GB) ([2.sup.36] bytes). The resolution of a bus address is a 32-byte **cache block** , which is the only unit of transfer supported. Consequently, 31 address bits suffice. One-quarter...

...CPUs do not store data from this region in their caches, and the target need **not** supply correct **ECC** bits.
The method used to select the target module of a bus operation is geographic...

18/3,K/42 (Item 10 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)

01496444 SUPPLIER NUMBER: 11745312 (USE FORMAT 7 OR 9 FOR FULL TEXT)
VAX 4000: the performance alternative. (DEC VAX 4000 minicomputer)
Pokorni, Miroslav
DEC Professional, v11, n1, p68(4)
Jan, 1992
ISSN: 0744-9216 LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 2779 LINE COUNT: 00208

...ABSTRACT: 4000. A technical discussion of memory architecture and access is presented. One way to improve **memory** performance is to apply fat **page** mode on interleaved **memory** ; another is to use an error-correcting circuit (**ECC**) to **avoid** memory read retries. Increasing the number of bits in the memory protection code improves data...

18/3,K/50 (Item 18 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)

01242821 SUPPLIER NUMBER: 06296634 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Cache chips score 32-bit MMU hits.
Cormier, Denny
ESD: The Electronic System Design Magazine, v18, n3, p21(2)
March, 1988
ISSN: 0893-2565 LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 1130 LINE COUNT: 00088

... the 132-pin [mu]PD43608 with a 32-bit CPU and its system bus include **bypass** , write, write- **check** , and **block** -load **buffers** . This additional hardware causes extra gate delays which can degrade performance, especially in multiprocessing applications...
?

File 348:EUROPEAN PATENTS 1978-2003/Dec W02
(c) 2003 European Patent Office
File 349:PCT FULLTEXT 1979-2002/UB=20031225,UT=20031218
(c) 2003 WIPO/Univentio
? ds

Set	Items	Description
S1	224155	PAGE OR PAGES
S2	457015	BLOCK? ?
S3	582707	STORAGE OR MEMORY OR BUFFER? ? OR CACHE? ? OR RAM OR ROM OR PROM OR EPROM OR FPROM OR CDROM? ?
S4	8302	EDAC OR ECC OR HAMMING
S5	6005	DEBUG? OR DE()BUG???? ?
S6	1811356	CHECK??? ? OR DETECT??? ? OR DIAGNOS???? ? OR DX OR ANALYZ? OR ANALYS? OR ANALYT? OR LOOK??? ? OR EXAMIN? OR SCREEN?
S7	734659	SCRUTIN? OR REVIEW? OR EVALUAT? OR INSPECT? OR MONITOR? OR TEST OR TESTS OR TESTED OR TESTING OR SCAN OR SCANS OR SCANNED OR SCANNING
S8	69904	('NOT' OR WITHOUT)(1W)S6:S7
S9	27235	UNCHECK? OR UNEXAMIN? OR UNSCREEN? OR UNSCRUTIN? OR UNREVIEW? OR UNEVALUAT? OR UNINSPECT? OR UNMONITOR? OR UNSCAN????? ? OR UNTEST??? ?
S10	1141	S4:S5(3N)('NOT' OR WITHOUT)
S11	532967	BYPASS? OR BY()PASS??? ? OR AVOID? OR SKIP???? ? OR IGNOR? OR DISREGARD? OR EXCLUD? OR EXCLUSION? OR PASS???()OVER
S12	0	'BY'()PASS??? ?
S13	23800	S11:S12(3N)S4:S7
S14	40188	S1:S2(5N)S3
S15	56206	S1:S2(10N)S3
S16	457	S15(25N)(S8:S10 OR S13)
S17	25	S16/TI,AB,CM
S18	5845	IC='H04L-009'
S19	8645	IC='G06F-011'
S20	43	S16 AND S18:S19
S21	66	S17 OR S20
S22	66	IDPAT (sorted in duplicate/non-duplicate order)
S23	66	IDPAT (primary/non-duplicate records only)

? t23/5,k/3,11-12,14,20

23/5,K/3 (Item 3 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

01474660
Semiconductor memory device, system, and method of controlling accessing to memory
Halbleiterspeicherbauelement, - system und Zugriffsverfahren
Dispositif de memoire semi-conductrice, son utilisation dans un systeme et procede d'acces
PATENT ASSIGNEE:
NEC CORPORATION, (236690), 7-1, Shiba 5-chome, Minato-ku, Tokyo, (JP), (Applicant designated States: all)
INVENTOR:
Shionoya, Shinichi, c/o NEC Corporation, 7-1, Shiba 5-chome, Minato-ku, Tokyo, (JP)
LEGAL REPRESENTATIVE:
Glawe. Delfs. Moll (100699), Patentanwalte Postfach 26 01 62, 80058 Munchen, (DE)
PATENT (CC, No, Kind, Date): EP 1251525 A1 021023 (Basic)
APPLICATION (CC, No, Date): EP 2002008850 020419;
PRIORITY (CC, No, Date): JP 2001120853 010419

DESIGNATED STATES: DE; GB
EXTENDED DESIGNATED STATES: AL; LT; LV; MK; RO; SI
INTERNATIONAL PATENT CLASS: G11C-029/00

ABSTRACT EP 1251525 A1
Test circuits 150)) to 154)), which determine whether memory blocks 110)) to 114)) including at least one redundant block are defective, are included in the memory blocks, respectively, A decoding rule generating circuit 13 so generates a decoding rule that a defective block can not be accessed, and outputs the generated decoding rule as a decoding-rule signal RUL. Under the decoding rule, the redundant address decoder 14 decodes the address signal ADDR, to permit access to the memory blocks except the defective block(s).
ABSTRACT WORD COUNT: 84
NOTE:
Figure number on first page: 1

LEGAL STATUS (Type, Pub Date, Kind, Text):

Application:	021023	A1	Published application with search report
Examination:	021113	A1	Date of request for examination: 20020909
Examination:	030305	A1	Date of dispatch of the first examination report: 20030116
Assignee:	030502	A1	Transfer of rights to new applicant: NEC Electronics Corporation (4260580) 1753 Shimonumabe, Nakahara-ku Kawasaki, Kanagawa 211-8668 JP

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	200243	377
SPEC A	(English)	200243	6134
Total word count - document A			6511
Total word count - document B			0
Total word count - documents A + B			6511

...CLAIMS of the plurality of memory blocks is defective;
generating a selecting rule for selecting accessible **memory blocks** , so that the one or more **memory block** (s) among the plurality of the **memory blocks** which is(are) determined as defective by said. **testing** will be **avoided** , while the at least one redundant **memory block** of the same number of the one or more **memory block** (s) determined as defective will be accessible;
selecting the accessible **memory blocks** , based on the selecting rule generated; and
accessing the accessible **memory blocks** to read/write data therefrom/thereto.

23/5,K/11 (Item 11 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

01053014
COMPRESSED MERGING OF RASTER IMAGES FOR HIGH SPEED DIGITAL PRINTING
MISCHUNG VON KOMPRIMIERTEN RASTERBILDERN IN EINEM DRUCKSYSTEM
FUSION DE TRAME-IMAGES COMPRIMEES DANS UN SYSTEME D'IMPRESSION
PATENT ASSIGNEE:
Esko-Graphics, (1912993), Tramstraat 69, 9052 Zwijnaarde, (BE),
(Proprietor designated states: all)
INVENTOR:

VLIETINCK, Jan, J., Galglaan 9, B-9000 Gent, (BE)
NOTREDAME, Paul, H., Klimoplaan 10, B-9032 Wondelgem, (BE)
DEBAERE, Eddy, H., Oudestraat 7A, B-9800 Deinze, (BE)
DEPUYDT, Lieven, W., Barco Patent Dept., Theodoor Sevenslaan 106, B-8500 Kortrijk, (BE)
LEGAL REPRESENTATIVE:
Bird, Ariane et al (76761), Bird Goen & Co, Klein Dalenstraat 42A, 3020 Winksele, (BE)
PATENT (CC, No, Kind, Date): EP 1057138 A1 001206 (Basic)
EP 1057138 B1 030806
WO 99024933 990520
APPLICATION (CC, No, Date): EP 98952450 981105; WO 98BE169 981105
PRIORITY (CC, No, Date): US 964651 971105
DESIGNATED STATES: DE
INTERNATIONAL PATENT CLASS: G06K-015/02; G06F-003/12
CITED PATENTS (EP B): EP 473340 A; EP 570146 A; EP 613102 A; EP 691784 A; US 4493049 A
CITED PATENTS (WO A): EP 570146 A ; US 4493049 A ; EP 473340 A ; EP 613102 A ; EP 691784 A
NOTE:
No A-document published by EPO
LEGAL STATUS (Type, Pub Date, Kind, Text):

Application:	001206 A1	Published application with search report
Application:	990721 A1	International application (Art. 158(1))
Grant:	030806 B1	Granted patent
Examination:	020619 A1	Date of dispatch of the first examination report: 20020502
Examination:	001206 A1	Date of request for examination: 20000828
Assignee:	030226 A1	Transfer of rights to new applicant: Esko-Graphics (1912993) Tramstraat 69 9052 Zwijnaarde BE

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS B	(English)	200332	2473
CLAIMS B	(German)	200332	2043
CLAIMS B	(French)	200332	2935
SPEC B	(English)	200332	22742
Total word count - document A			0
Total word count - document B			30193
Total word count - documents A + B			30193

...CLAIMS obtains the line work compressed data and the CT compressed data as required by the **page** layout script from the **page** element **cache** .
36. The system according to any of claims 33 to 35 wherein the compressed rasterized page element data is **unscreened** .
37. The system according to any of claims 33 to 36 wherein the compressed rasterized...

23/5,K/12 (Item 12 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

01029512
A multi-processor computer system and a method of operating thereof
Multiprozessor-Rechnersystem und Verfahren zu seinem Betrieb
Systeme d'ordinateur multiprocesseur et procede pour son fonctionnement
PATENT ASSIGNEE:
Compaq Computer Corporation, (687792), 20555 S.H. 249, Houston Texas

77070, (US), (Applicant designated States: all)
INVENTOR:
Noel, Karen, 238 Academy Road, Pembroke, NH 03275, (US)
Benson, Thomas, 14 Summer Lane, Hollis, NH 03049, (US)
Jordan, Gregory H., 22 Jambard Road, Hollis, NH 03049, (US)
Kauffman, James R., 31 Norma Drive, Nashua, NH 03062, (US)
Mason, Andrew H., 61 Baxter Road, Hollis, NH 03049, (US)
Harter, Paul K., 63 Whiley Road, Groton, MA 01450, (US)
Bishop, Richard A., 1 Mullikin Road, Merrimack, NH 03054, (US)
Kleinsorge, Frederick G., 4 Farmington Road, Amherst, NH 03031, (US)
Shirron, Stephen, 123 Parker Street, Acton, MA 01720, (US)
Zalewski, Stephen, 17306 NE 129th Street, Redmond, WA 98052, (US)
LEGAL REPRESENTATIVE:
Brunner, Michael John (28871), GILL JENNINGS & EVERY Broadgate House 7 Eldon Street, London EC2M 7LH, (GB)
PATENT (CC, No, Kind, Date): EP 917056 A2 990519 (Basic)
EP 917056 A3 000809
APPLICATION (CC, No, Date): EP 98309006 981104;
PRIORITY (CC, No, Date): US 64250 971104; US 95368 980610; US 95265 980610; US 95521 980610; US 95188 980610; US 90027 980610; US 95543 980610; US 95379 980610; US 95277 980610; US 95266 980610; US 95264 980610; US 95256 980610
DESIGNATED STATES: DE; FR; GB
EXTENDED DESIGNATED STATES: AL; LT; LV; MK; RO; SI
INTERNATIONAL PATENT CLASS: G06F-009/46

ABSTRACT EP 917056 A2
A computer system has a plurality of assignable system resources, induding processors, memory and I/O circuitry; an interconnection mechanism for electrically interconnecting the processors, memory and I/O circuitry so that each processor has electrical access to all the memory and at least some of the I/O circuitry; a software mechanism for assigning the assignable system resources to a plurality of partitions, each partition including at least one processor, some memory and some I/O circuitry; and an operating system instance running in each partition. The computer system provides improved flexibility, resource availability, resource migration capabilities and scalability.
ABSTRACT WORD COUNT: 97
NOTE:
Figure number on first page: 2

LEGAL STATUS (Type, Pub Date, Kind, Text):
Assignee: 000517 A2 Transfer of rights to new applicant: Compaq Computer Corporation (687792) 20555 S.H. 249 Houston Texas 77070 US
Application: 990519 A2 Published application (Alwith Search Report ;A2without Search Report)
Search Report: 000809 A3 Separate publication of the search report
Examination: 010321 A2 Date of request for examination: 20010122
LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	9920	3274
SPEC A	(English)	9920	43298
Total word count - document A			46572
Total word count - document B			0
Total word count - documents A + B			46572

...CLAIMS A computer system according to claim 16 wherein the software mechanism (A) maintains free, zeroed, **untested** , and bad **memory page** lists; and **memory pages** to be removed are modified to an

unowned status if they are on any of the **memory page** lists; (B) maintains a modified **page** list that indicates those **memory pages** which have been modified, but not written to a system paging file; and (C) maintains...

23/5,K/14 (Item 14 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00954215
Method for analyzing computer performance data
Verfahren zur Analyse von Computerleistungsdaten
Procede pour l'analyse des donnees relatives a la performance d'un ordinateur
PATENT ASSIGNEE:
DIGITAL EQUIPMENT CORPORATION, (313085), 111 Powdermill Road, Maynard, Massachusetts 01754, (US), (Applicant designated States: all)
INVENTOR:
Henzinger, Monika H., 80 La Loma Drive, Menlo Park, California, (US)
Vandevoorde, Mark T., 1159 Corral Avenue, Sunnyvale, California 94086, (US)
Weihl, William, 280 Clipper Street, San Francisco, California 94114, (US)
Sites, Richard L., 145 Campo Bello Lane, Menlo Park, California 94025, (US)
Leung, Shun-Tak Albert, 1285 Montecito Avenue, No. 24, Mountain View, California 94043, (US)
LEGAL REPRESENTATIVE:
Charig, Raymond Julian (79692), Eric Potter Clarkson, Park View House, 58 The Ropewalk, Nottingham NG1 5DD, (GB)
PATENT (CC, No, Kind, Date): EP 864980 A2 980916 (Basic)
EP 864980 A3 000405
APPLICATION (CC, No, Date): EP 98301588 980304;
PRIORITY (CC, No, Date): US 814190 970310
DESIGNATED STATES: AT; BE; CH; DE; DK; ES; FI; FR; GB; GR; IE; IT; LI; LU; MC; NL; PT; SE
EXTENDED DESIGNATED STATES: AL; LT; LV; MK; RO; SI
INTERNATIONAL PATENT CLASS: **G06F-011/34** ; G06F-009/38; G06F-009/45

ABSTRACT EP 864980 A2
In a computerized method, performance data collected while a computer system executed instructions of a program are analyzed. The method collects performance data while executing the program. The performance data includes sample counts of instructions executed. The program is analyzed to determine classes of instructions.
Instructions of the same equivalence class all execute the identical number of times. The execution frequencies for each instruction of each equivalence class is estimated. The estimated execution frequencies can then be used to the average number of cycles required to issue each instruction of each equivalence class. The average number of cycles can be compared with the minimum number of cycles to determine the number of dynamic stall cycles incurred by the instructions. Furthermore, reasons for the dynamic stall cycles can be inferred.
ABSTRACT WORD COUNT: 130
NOTE:
Figure number on first page: 15

LEGAL STATUS (Type, Pub Date, Kind, Text):
Withdrawal: 010411 A2 Date application deemed withdrawn: 20001003
Change: 20000112 A2 International Patent Classification changed: 19991120

Application: 980916 A2 Published application (A1with Search Report ;A2without Search Report)
Search Report: 20000405 A3 Separate publication of the search report
LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	9838	992
SPEC A	(English)	9838	13552
Total word count - document A			14544
Total word count - document B			0
Total word count - documents A + B			14544

INTERNATIONAL PATENT CLASS: **G06F-011/34** ...

...SPECIFICATION the same cache line if their addresses produce the same quotient when divided by the **cache** line size. This **analysis** may **ignore** predecessor **blocks** which are executed much less often than the basic block containing the stalled instruction, according...

23/5,K/20 (Item 20 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00726077
Emulation device, system and method with distributed control of test interfaces in clock domains.
Vorrichtung, System und Verfahren zur Emulation mit dezentraler Steuerung im Taktbereich-Prufungsschnittsteller.
Dispositif, systeme et procede d'emulation avec commande decentralisee d'interface de test.
PATENT ASSIGNEE:
TEXAS INSTRUMENTS INCORPORATED, (279070), 13500 North Central Expressway, Dallas Texas 75265, (US), (applicant designated states: DE;FR;GB;IT;NL)
INVENTOR:
Swoboda, Gary L., 4435 Balboa, Sugar Land, TX 77479, (US)
LEGAL REPRESENTATIVE:
Nettleton, John Victor et al (34281), Abel & Imray Northumberland House 303-306 High Holborn, London, WC1V 7LH, (GB)
PATENT (CC, No, Kind, Date): EP 685793 A2 951206 (Basic)
EP 685793 A3 990303
APPLICATION (CC, No, Date): EP 95301531 950309;
PRIORITY (CC, No, Date): US 208543 940309; US 209127 940309; US 208469 940309
DESIGNATED STATES: DE; FR; GB; IT; NL
INTERNATIONAL PATENT CLASS: **G06F-011/26** ; G01R-031/3185

ABSTRACT EP 685793 A2
An emulation device (11) distributes common control information (8801) to each of a plurality of clock domains (1213,1215, 1217) into which the emulation device is partitioned, and also provides the clock domains with individualized clock control (8905, 8907, 8913). (see image in original document)
ABSTRACT WORD COUNT: 46

LEGAL STATUS (Type, Pub Date, Kind, Text):
Withdrawal: 000524 A2 Date application deemed withdrawn: 19990904
Application: 951206 A2 Published application (A1with Search Report ;A2without Search Report)
Search Report: 990303 A3 Separate publication of the European or

International search report
Change: 990310 A2 Obligatory supplementary classification (change)
LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	EPAB95	689
SPEC A	(English)	EPAB95	34725
Total word count - document A			35414
Total word count - document B			0
Total word count - documents A + B			35414

INTERNATIONAL PATENT CLASS: **G06F-011/26** ...

...SPECIFICATION in cache without being affected by functional host computer HCF of Fig. 80. This bit **blocks** reset, all interrupts, and the **cache** enable bit. The **cache** P flags are **not checked** during Macro mode, and can be cleared by the host HCF. When reloading the cache...
? t23/5,k/21,24,28,31,33

23/5,K/21 (Item 21 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00700335
A method and apparatus for detecting memory access errors.
Verfahren und Einrichtung zum Nachweis von Speicherzugriffsfehlern.
Procede et appareil pour detecter des erreurs d'acces a la memoire.
PATENT ASSIGNEE:
AT&T Corp., (589370), 32 Avenue of the Americas, New York, NY 10013-2412, (US), (applicant designated states: DE;FR;GB)
INVENTOR:
Goodnow II, James E., 12477 Old Mine Road, Grass Valley, CA 95945, (US)
Kowalski, Thaddeus Julius, 73 Stoneridge Road, Summit, NJ 07901, (US)
Rowland, James R., 18 Thackeray Drive, Short Hills, NJ 07078, (US)
LEGAL REPRESENTATIVE:
Watts, Christopher Malcolm Kelway, Dr. et al (37391), AT&T (UK) Ltd. 5, Mornington Road, Woodford Green Essex, IG8 0TU, (GB)
PATENT (CC, No, Kind, Date): EP 666535 A2 950809 (Basic)
EP 666535 A3 960228
APPLICATION (CC, No, Date): EP 95300460 950126;
PRIORITY (CC, No, Date): US 192239 940204
DESIGNATED STATES: DE; FR; GB
INTERNATIONAL PATENT CLASS: G06F-011/00 ; G06F-009/45
ABSTRACT EP 666535 A2
Disclosed is a software generation system (SGS) based memory error detection system which may be utilized to detect various memory access errors, such as array dimension violations, dereferencing of invalid pointers, accessing freed memory, reading uninitialized memory, and automated detection of memory leaks. Error checking commands and additional information are inserted into a parse tree associated with a source code file being tested at read-time which serve to initiate and facilitate run-time error detection processes. Wrapper functions may be provided for initiating error checking processes for associated library functions. A pointer check table maintains pointer information, including valid range information, for each pointer that is utilized to monitor the use and modification of the respective pointers. A memory allocation structure records allocation information, including a chain list of all pointers that point to the memory region and an initialization status for each byte in the memory region, for each region of memory. The chain list is utilized to monitor the deallocation

of the associated memory region, as well as to detect when there is a memory leak. The initialization status is used to ensure that a region of uninitialized memory is not accessed. A data flow analysis algorithm minimizes the number of pointer checks that have to be performed and allows certain read-time errors to be detected. (see image in original document)
ABSTRACT WORD COUNT: 254

LEGAL STATUS (Type, Pub Date, Kind, Text):

Application:	950809	A2	Published application (Alwith Search Report ;A2without Search Report)
Change:	960214	A2	Obligatory supplementary classification (change)
Search Report:	960228	A3	Separate publication of the European or International search report
Examination:	961023	A2	Date of filing of request for examination: 960819
Examination:	971008	A2	Date of despatch of first examination report: 970822
Withdrawal:	971203	A2	Date on which the European patent application was withdrawn: 971006

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	EPAB95	5367
SPEC A	(English)	EPAB95	18095
Total word count - document A			23462
Total word count - document B			0
Total word count - documents A + B			23462

INTERNATIONAL PATENT CLASS: **G06F-011/00** ...

...SPECIFICATION Purify(TM) system provides an effective basis for detecting many memory access errors, it will **not detect** the common programming error that occurs when a pointer associated with a first **block** of allocated **memory** incorrectly accesses a second **block** of allocated and initialized **memory** . The Purify(TM) system will only verify that the memory pointed to by a pointer...

23/5,K/24 (Item 24 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00662617
Image communication apparatus having storage unit for storing recorded sheet
Bildkommunikationsgerat mit Einheit zur Speicherung von Aufzeichnungspapier
Appareil de communication d'image ayant une unite de rangement pour stocker des feuilles d'enregistrement
PATENT ASSIGNEE:
CANON KABUSHIKI KAISHA, (542361), 30-2, 3-chome, Shimomaruko, Ohta-ku, Tokyo, (JP), (Proprietor designated states: all)
INVENTOR:
Matsumoto, Hiroaki, c/o Canon K.K., 30-2, 3-chome, Shimomaruko, Ohta-ku, Tokyo 146, (JP)
Sobue, Ikuo, c/o Canon K.K., 30-2, 3-chome, Shimomaruko, Ohta-ku, Tokyo 146, (JP)
Ejiri, Seishi, c/o Canon K.K., 30-2, 3-chome, Simomaruko, Ohta-ku, Tokyo 146, (JP)

Kiguchi, Masao, c/o Canon K.K., 30-2, 3-chome, Simomaruko, Ohta-ku, Tokyo 146, (JP)
Ishizuka, Haruo, c/o Canon K.K., 30-2, 3-chome, Simomaruko, Ohta-ku, Tokyo 146, (JP)
Matsumoto, Yasuhiro, c/o Canon K.K., 30-2, 3-chome, Simomaruko, Ohta-ku, Tokyo 146, (JP)
Nakayama, Yoshiyuki, c/o Canon K.K., 30-2, 3-chome, Simomaruko, Ohta-ku, Tokyo 146, (JP)
LEGAL REPRESENTATIVE:
Tiedtke, Harro, Dipl.-Ing. (11949), Patentanwaltsburo Tiedtke-Buhling-Kinne & Partner Bavariaring 4, 80336 Munchen, (DE)
PATENT (CC, No, Kind, Date): EP 637164 A2 950201 (Basic)
EP 637164 A3 950628
EP 637164 B1 000126
APPLICATION (CC, No, Date): EP 94111868 940729;
PRIORITY (CC, No, Date): JP 93208749 930731; JP 93208754 930731; JP 93340014 931206; JP 93340019 931206
DESIGNATED STATES: DE; ES; FR; GB; IT
INTERNATIONAL PATENT CLASS: H04N-001/00
CITED PATENTS (EP B): US 4995602 A; US 5003627 A; US 5229827 A
CITED REFERENCES (EP B):
PATENT ABSTRACTS OF JAPAN vol. 15 no. 396 (M-1166) ,8 October 1991 & JP-A-03 162365 (CANON) 12 July 1991,
PATENT ABSTRACTS OF JAPAN vol. 012 no. 397 (E-672) ,21 October 1988 & JP-A-63 138883 (TOSHIBA CORP) 10 June 1988,
PATENT ABSTRACTS OF JAPAN vol. 14 no. 164 (M-0957) ,30 March 1990 & JP-A-02 023157 (IKEGAMI TSUSHINKI) 25 January 1990,
PATENT ABSTRACTS OF JAPAN vol. 006 no. 238 (E-144) ,26 November 1982 & JP-A-57 136865 (FUJITSU KK) 24 August 1982,
PATENT ABSTRACTS OF JAPAN vol. 007 no. 272 (E-214) ,3 December 1983 & JP-A-58 151770 (NIPPON DENKI KK) 9 September 1983,
PATENT ABSTRACTS OF JAPAN vol. 007 no. 189 (M-237) ,18 August 1983 & JP-A-58 089558 (CANON KK) 27 May 1983,;

ABSTRACT EP 637164 A2
An image communication apparatus includes a reception unit for receiving image data, a first controller for storing the image data received by the reception unit in a memory, and counting the page number the reception image data, a recording unit for recording an image on a sheet on the basis of the image data stored in the memory, a storage unit having a plurality of trays for sorting and storing sheets on which images are recorded by the recording unit, the plurality of trays having a first tray having a small sheet stackable number and a second tray having a large sheet stackable number, and a second controller for selecting the first tray when the page number counted by the first controller is equal to or smaller than a predetermined page number, and selecting the second tray when the counted page number is larger than the predetermined page number, thereby storing the sheets. (see image in original document)
ABSTRACT WORD COUNT: 160
NOTE:
Figure number on first page: 1

LEGAL STATUS (Type, Pub Date, Kind, Text):

Oppn None:	010110 B1	No opposition filed: 20001027
Grant:	20000126 B1	Granted patent
Lapse:	020626 B1	Date of lapse of European Patent in a contracting state (Country, date): ES 20000126, FR 20000623,
Lapse:	010228 B1	Date of lapse of European Patent in a contracting state (Country, date): FR

		20000623,
Application:	950201 A2	Published application (A1with Search Report ;A2without Search Report)
Search Report:	950628 A3	Separate publication of the European or International search report
Examination:	960110 A2	Date of filing of request for examination: 951114
Examination:	980722 A2	Date of despatch of first examination report: 980604
Change:	990421 A2	Title of invention (German) (change)
Change:	990421 A2	Title of invention (English) (change)
Change:	990421 A2	Title of invention (French) (change)
Change:	990428 A2	Title of invention (German) (change)
Change:	990428 A2	Title of invention (English) (change)
Change:	990428 A2	Title of invention (French) (change)

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS B	(English)	200004	459
CLAIMS B	(German)	200004	400
CLAIMS B	(French)	200004	519
SPEC B	(English)	200004	11874
Total word count - document A			0
Total word count - document B			13252
Total word count - documents A + B			13252

23/5,K/28 (Item 28 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00545380
Write through virtual cache memory, alias addressing, and cache flushes
Virtueller Durchschreibcachespeicher Synonym-Adressierung und Cache-Ungultigkeitserklarungen
Antememoire virtuelle a ecriture au travers, adressage de synonymes et invalidations d'antememoire
PATENT ASSIGNEE:
SUN MICROSYSTEMS, INC., (1392730), 2550 Garcia Avenue, Mountain View, CA 94043, (US), (applicant designated states: DE;FR;GB;IT;NL)
INVENTOR:
Young, Mark, 2343, Perich Court, Mountain View, California 94040, (US)
LEGAL REPRESENTATIVE:
Wombwell, Francis (46021), Potts, Kerr & Co. 15, Hamilton Square, Birkenhead Merseyside L41 6BR, (GB)
PATENT (CC, No, Kind, Date): EP 541319 A1 930512 (Basic)
EP 541319 B1 970502
APPLICATION (CC, No, Date): EP 92310027 921102;
PRIORITY (CC, No, Date): US 787547 911104
DESIGNATED STATES: DE; FR; GB; IT; NL
INTERNATIONAL PATENT CLASS: G06F-012/10; G06F-012/08;
CITED PATENTS (EP A): EP 322888 A
CITED REFERENCES (EP A):
CONFERENCE ON COMPUTER WORKSTATIONS vol. 2, 1988, IEEE, NEW YORK ,US pages 80 - 87 FRINK ET AL. 'A virtual cache-based workstation architecture';

ABSTRACT EP 541319 A1
In a computer system comprising a CPU, a cache memory and a main memory wherein the cache memory is virtually addressed, and some of the virtual addresses are alias address to each other, a cache memory controller

comprising a cache control logic, a cache tag array, a memory management unit, and an alias detection logic is provided. The cache control logic skips flushing of a cache line if the cache line is corresponding to a memory block in a non-cacheable physical memory page, thereby avoiding unnecessary flushes and allowing the CPU to update the cache memory and the main memory using an improved write through and no write allocate approach that reduces cache flushes. (see image in original document)
ABSTRACT WORD COUNT: 121

LEGAL STATUS (Type, Pub Date, Kind, Text):
Application: 930512 A1 Published application (Alwith Search Report ;A2without Search Report)
Examination: 931222 A1 Date of filing of request for examination: 931021
Examination: 940302 A1 Date of despatch of first examination report: 940112
Grant: 970502 B1 Granted patent
Oppn None: 980422 B1 No opposition filed
LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS B	(English)	EPAB97	1062
CLAIMS B	(German)	EPAB97	912
CLAIMS B	(French)	EPAB97	1338
SPEC B	(English)	EPAB97	2658
Total word count - document A			0
Total word count - document B			5970
Total word count - documents A + B			5970

...CLAIMS memory if said main memory location identified by said physical address is a non-cacheable **memory** location of a non-cacheable **memory block** of said main **memory** the result of said non-cacheability being available after the result of said cache hit/miss determination; and characterized by conditionally flushing, **without detecting** for alias addresses of said virtual address, by said **cache memory** a **cache** line in which said **memory block** could have been **cached** if said virtual address results in said write cache miss and said memory location is...

...hit/miss determination,
and characterized by said cache control logic comprising means for conditionally flushing, **without detecting** for alias address of said virtual address, a **cache** line in which said **memory block** could have been **cached** if said virtual address results in said write cache miss and said memory location is...

23/5,K/31 (Item 31 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00471228
Testable RAM architecture in a microprocessor having embedded cache memory
Prufbare RAM-Architektur in einem Mikroprozessor mit eingebettetem Cache-Speicher
Architecture de RAM testable dans un microprocesseur ayant une antememoire encastree
PATENT ASSIGNEE:
LSI LOGIC CORPORATION, (561302), 1551 McCarthy Boulevard, Milpitas, CA 95035, (US), (applicant designated states: DE;FR;GB;IT;NL)

INVENTOR:
Fuccio, Michael, 2448 Rockridge Way, Santa Clara, California 95051, (US)
Desai, Sanjay, 751 Mahogany Lane, Sunnyvale, California 94086, (US)
LEGAL REPRESENTATIVE:
Kahler, Kurt, Dipl.-Ing. (6167), Patentanwalte Kahler, Kack, Fiener et col., Vorderer Anger 268, 86899 Landsberg/Lech, (DE)
PATENT (CC, No, Kind, Date): EP 480421 A2 920415 (Basic)
EP 480421 A3 930421
EP 480421 B1 970709
APPLICATION (CC, No, Date): EP 91117293 911010;
PRIORITY (CC, No, Date): US 596986 901012
DESIGNATED STATES: DE; FR; GB; IT; NL
INTERNATIONAL PATENT CLASS: **G06F-011/267** ; G06F-012/08; G11C-029/00
CITED PATENTS (EP A): US 4744049 A; US 4562536 A
CITED REFERENCES (EP A):
INT'L TEST CONFERENCE, WASHINGTON D.C., US SEPTEMBER 1-3, 1987, L. BASTO ET AL: 'Testing the MC68030 Caches', pp826-833
INT'L TEST CONFERENCE, WASHINGTON D.C., US SEPTEMBER 10-14, 1990, M. G. GALLUP ET AL: 'Testability Features of the 68040', pp749-757
IEEE INTERNATIONAL SOLID STATE CIRCUITS CONFERENCE vol. 30, February 1987, NEW YORK US pages 32 - 33 , XP211630 D. ARCHER ET AL 'A 32b CMOS Microprocesor with On-Chip Instruction and Data Caching and Memory Management';

ABSTRACT EP 480421 A2
A microprocessor (100) with embedded cache memory (204) is disclosed. In a "test mode" of operation, caches (204) are accessed directly from the memory interface signals. Direct writing and reading to/from the instruction and data caches (204) allows the testing of the functionality of the cache memory arrays (204). External memory interface is granted to an external master via a bus arbitration mechanism so that the test mode operation can be utilized. (see image in original document)
ABSTRACT WORD COUNT: 79

LEGAL STATUS (Type, Pub Date, Kind, Text):

Application:	920415	A2	Published application (A1with Search Report ;A2without Search Report)
Search Report:	930421	A3	Separate publication of the European or International search report
Examination:	931222	A2	Date of filing of request for examination: 931021
Examination:	960207	A2	Date of despatch of first examination report: 951227
Change:	960626	A2	Representative (change)
Grant:	970709	B1	Granted patent
Oppn None:	980701	B1	No opposition filed

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	EPABF1	311
CLAIMS B	(English)	EPAB97	295
CLAIMS B	(German)	EPAB97	318
CLAIMS B	(French)	EPAB97	367
SPEC A	(English)	EPABF1	4542
SPEC B	(English)	EPAB97	4867
Total word count - document A			4853
Total word count - document B			5847
Total word count - documents A + B			10700

INTERNATIONAL PATENT CLASS: **G06F-011/267** ...

...SPECIFICATION 428, and a stall request is issued to the CPU in the test

mode.

A **Memory Block** Queue (MBQUEUE) **block** 403 maintains information pertaining to external **memory** access, including a) an external memory start bit, which is **bypassed** in the **test** mode, b) an instruction/data transaction bit for selecting ICache or DCache, c) a cacheable...

...SPECIFICATION 428, and a stall request is issued to the CPU in the test mode.

A **Memory Block** Queue (MBQUEUE) 1block 403 maintains information pertaining to external **memory** access, including a) an external memory start bit, which is **bypassed** in the **test** mode, b) an instruction/data transaction bit for selecting ICache or DCache, c) a cacheable...

23/5,K/33 (Item 33 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00435168
Method and system for dynamically controlling the operation of a program
Verfahren und System zur dynamischen Programmbetriebssteuerung
Procede et systeme de commande dynamique du fonctionnement d'un programme
PATENT ASSIGNEE:
DATA GENERAL CORPORATION, (410941), 4400 Computer Drive, Westboro Massachusetts 01580, (US), (applicant designated states: DE;FR;GB)
INVENTOR:
Kelley, Michael Halstead, 605, Merwin Road, Raleigh, North Carolina 27606, (US)
LEGAL REPRESENTATIVE:
Abnett, Richard Charles et al (27531), REDDIE & GROSE 16 Theobalds Road, London WC1X 8PL, (GB)
PATENT (CC, No, Kind, Date): EP 424031 A2 910424 (Basic)
EP 424031 A3 920304
EP 424031 B1 960911
APPLICATION (CC, No, Date): EP 90311166 901011;
PRIORITY (CC, No, Date): US 424184 891019
DESIGNATED STATES: DE; FR; GB
INTERNATIONAL PATENT CLASS: **G06F-011/00** ; **G06F-011/14**
CITED PATENTS (EP A): WO 8402410 A; WO 8402410 A; EP 212791 A; EP 212791 A

ABSTRACT EP 424031 A2

In a data processing system, the time lost in checking for the presence of all memory references required byl a special section of code before the program is run is substantially reduced, and the program requiring the memory reference is dynamically protected from crashing if the memory reference is not presently available. The method assumes that all memory references are available and begins running (45) the special section of code **without checking** their availability. If a request is made for information that is not in assigned **memory storage** , a **page** fault occurs (47), and the data processing system interrupts the running of the special section of code (37) and undoes everything the special section of code has done prior to the interrupt (39). The requested memory reference is then located in storage (41), and the information is retrieved and written into assigned memory (43). The special section of code is then restarted and will now be supplied with the needed information. It has been found that in practice it takes much less time to assume the memory references will be present and occasionally interrupt, erase and restart, than to make a preliminary check for all memory references. (see image in original document)
ABSTRACT WORD COUNT: 206

LEGAL STATUS (Type, Pub Date, Kind, Text):
 Application: 910424 A2 Published application (Alwith Search Report ;A2without Search Report)
 Search Report: 920304 A3 Separate publication of the European or International search report
 Examination: 920826 A2 Date of filing of request for examination: 920629
 Examination: 950322 A2 Date of despatch of first examination report: 950208
 Grant: 960911 B1 Granted patent
 Oppn None: 970903 B1 No opposition filed
LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:
Available Text Language Update Word Count
CLAIMS B (English) EPAB96 654
CLAIMS B (German) EPAB96 561
CLAIMS B (French) EPAB96 705
SPEC B (English) EPAB96 1895
Total word count - document A 0
Total word count - document B 3815
Total word count - documents A + B 3815
INTERNATIONAL PATENT CLASS: **G06F-011/00** ...

... **G06F-011/14**

...ABSTRACT that all memory references are available and begins running (45) the special section of code **without checking** their availability. If a request is made for information that is not in assigned **memory storage** , a **page** fault occurs (47), and the data processing system interrupts the running of the special section...
? t23/5,k/34,51

23/5,K/34 (Item 34 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00430529
Fault tolerant data processing system initialisation
Initialisation eines fehlertoleranten Datenverarbeitungssystems
Initialisation d'un systeme de traitement de donnees a tolerance de fautes
PATENT ASSIGNEE:
International Business Machines Corporation, (200120), Old Orchard Road, Armonk, N.Y. 10504, (US), (applicant designated states: AT;BE;CH;DE;DK;ES;FR;GB;GR;IT;LI;LU;NL;SE)
INVENTOR:
Freeman, Bobby Joe, 1381 S.W. 28th Avenue, Boynton Beach, FL 33426, (US)
Dinwiddie, John Monroe, Jr., 112 Pacer Circle, West Palm Beach, FL 33414, (US)
Grice, Lonnie Edward, 252 N.W. 44th Street, Boca Raton, FL 33431, (US)
Loffredo, John Mario, 2694 S.W. 14th Drive, Deerfield Beach, FL 33442, (US)
Sanderson, Kenneth Russell, 1132 Widgeon Road, West Palm Beach, FL 33414, (US)
Suarez, Gustavo Armando, 21482 Woodchuck Lane, Boca Raton, FL 33428, (US)
LEGAL REPRESENTATIVE:
Bailey, Geoffrey Alan (27921), IBM United Kingdom Limited Intellectual Property Department Hursley Park, Winchester Hampshire SO21 2JN, (GB)
PATENT (CC, No, Kind, Date): EP 405736 A2 910102 (Basic)
EP 405736 A3 940202
EP 405736 B1 971217

APPLICATION (CC, No, Date): EP 90305310 900516;
PRIORITY (CC, No, Date): US 353112 890517
DESIGNATED STATES: AT; BE; CH; DE; DK; ES; FR; GB; GR; IT; LI; LU; NL; SE
INTERNATIONAL PATENT CLASS: **G06F-011/16** ; G06F-009/44; G06F-015/177
CITED PATENTS (EP A): US 4816990 A; US 4812975 A; EP 197499 A; US 3950729 A ; EP 132157 A; EP 205949 A; US 4315310 A
CITED REFERENCES (EP A):
IBM TECHNICAL DISCLOSURE BULLETIN vol. 26, no. 11 , April 1984 , ARMONK, USA pages 5917 - 5918 R.L. COOK ET AL. 'MULTIPROCESSING WITH DISSIMILAR PROCESSORS';

ABSTRACT EP 405736 A2

The functions of two virtual operating systems (e.g. S/370 VM, VSE or IX370 and S/88 OS) are merged into one physical system. Partner pairs of S/88 processors run the S/88 OS and handle the fault tolerant and single system image aspects of the system. One or more partner pairs of S/370 processors are coupled to corresponding S/88 processors directly and through the S/88 bus. Each S/370 processor is allocated form 1 to 16 megabytes of contiguous storage from the S/88 main storage. Each S/370 virtual operating system thinks its memory allocation starts at address 0, and it manages its memory through normal S/370 dynamic memory allocation and paging techniques. The S/370 is limit checked to prevent the S/370 from accessing S/88 memory space. The S/88 Operating System is the master over all system hardware and I/O devices. The S/88 processors across the S/370 address space in direct response to a S/88 application program so that the S/88 may move I/O data into the S/370 I/O buffers and process the S/370 I/O operations. The S/88 and S/370 peer processor pairs to execute their respective Operating Systems in a single system environment without significant rewriting of either operating system. Neither operating system is aware of the other operating system nor the other processor pairs. (see image in original document)
ABSTRACT WORD COUNT: 219

LEGAL STATUS (Type, Pub Date, Kind, Text):

Lapse:	020612 B1	Date of lapse of European Patent in a contracting state (Country, date): AT 19971217, BE 19971217, CH 19971217, LI 19971217, ES 19971217, FR 19980515, GR 19971217, LU 19980531, SE 19980317,
Lapse:	20000126 B1	Date of lapse of European Patent in a contracting state (Country, date): AT 19971217, BE 19971217, CH 19971217, LI 19971217, FR 19980515, GR 19971217, SE 19980317,
Lapse:	030212 B1	Date of lapse of European Patent in a contracting state (Country, date): AT 19971217, BE 19971217, CH 19971217, LI 19971217, ES 19971217, FR 19980515, GR 19971217, LU 19980531, NL 19971217, SE 19980317,
Application:	910102 A2	Published application (A1with Search Report ;A2without Search Report)
Lapse:	20000209 B1	Date of lapse of European Patent in a contracting state (Country, date): AT 19971217, BE 19971217, CH 19971217, LI 19971217, FR 19980515, GR 19971217, LU 19980531, SE 19980317,
Examination:	910206 A2	Date of filing of request for examination: 901213
Change:	940126 A2	Obligatory supplementary classification (change)

Search Report:	940202 A3	Separate publication of the European or International search report
Examination:	960522 A2	Date of despatch of first examination report: 960403
Grant:	971217 B1	Granted patent
Lapse:	980826 B1	Date of lapse of the European patent in a Contracting State: SE 980317
Lapse:	980930 B1	Date of lapse of the European patent in a Contracting State: AT 971217, SE 980317
Lapse:	981021 B1	Date of lapse of the European patent in a Contracting State: AT 971217, CH 971217, LI 971217, SE 980317
Lapse:	981021 B1	Date of lapse of the European patent in a Contracting State: AT 971217, CH 971217, LI 971217, SE 980317
Lapse:	981028 B1	Date of lapse of the European patent in a Contracting State: AT 971217, CH 971217, LI 971217, FR 980515, SE 980317
Lapse:	981111 B1	Date of lapse of the European patent in a Contracting State: AT 971217, BE 971217, CH 971217, LI 971217, FR 980515, SE 980317
Oppn None:	981209 B1	No opposition filed

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS B	(English)	9712W2	701
CLAIMS B	(German)	9712W2	620
CLAIMS B	(French)	9712W2	806
SPEC B	(English)	9712W2	71242
Total word count - document A			0
Total word count - document B			73369
Total word count - documents A + B			73369

INTERNATIONAL PATENT CLASS: **G06F-011/16** ...

23/5,K/51 (Item 51 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00972261 **Image available**
METHOD AND APPARATUS FOR PRESERVATION OF FAILURE STATE IN A READ DESTRUCTIVE MEMORY
PROCEDE ET DISPOSITIF DE PRESERVATION D'UN ETAT D'ECHEC DANS UNE MEMOIRE A LECTURE DESTRUCTIVE

Patent Applicant/Assignee:
INTEL CORPORATION, 2200 Mission College Boulevard, Santa Clara, CA 95052, US, US (Residence), US (Nationality), (For all designated states except: US)
Patent Applicant/Inventor:
GARNEY John I, 8711 NW Benson Street, Portland, OR 97229, US, US (Residence), US (Nationality), (Designated only for: US)
COULSON Richard, 17454 NW Gilbert Lane, Portland, OR 97229, US, US (Residence), US (Nationality), (Designated only for: US)
FABER Robert W, 942 NE Third Avenue, Hillsboro, OR 97124, US, US (Residence), US (Nationality), (Designated only for: US)
Legal Representative:
MALLIE Michael J (agent), Blakely, Sokoloff, Taylor & Zafman, 7th Floor, 12400 Wilshire Boulevard, Los Angeles, CA 90025, US,
Patent and Priority Information (Country, Number, Date):
Patent: WO 200301380 A2-A3 20030103 (WO 0301380)

Application: WO 2002US18174 20020607 (PCT/WO US0218174)
Priority Application: US 2001888123 20010622
Designated States: AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ OM PH PL PT RO RU SD SE SG SI SK SL TJ TM TN TR TT TZ UA UG US UZ VN YU ZA ZM ZW
(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR
(OA) BF BJ CF CG CI CM GA GN GQ GW ML MR NE SN TD TG
(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZM ZW
(EA) AM AZ BY KG KZ MD RU TJ TM
Main International Patent Class: **G06F-011/00**
Publication Language: English
Filing Language: English
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 3825

English Abstract
One aspect of the invention provides a novel scheme to preserve the failure state of a memory location. According to one embodiment, the data is read from a memory location in a read-destructive memory device. If the data is found to be valid (uncorrupted) it is written back to the memory location from where it was read in order to preserve it. If the data is found to be invalid (corrupted) then a failure codeword is written in the memory location to indicate a failure of the memory location. The failure codeword may be preselected or dynamically calculated so that it has a mathematical distance greater than all correctable data patterns.

French Abstract
Un aspect de l'invention concerne un nouveau programme destine a preserver l'etat d'echec d'un emplacement memoire. Selon un mode de realisation, les donnees sont lues a partir d'un emplacement memoire dans une memoire a lecture destructive. Si les donnees sont valides (non corrompues), elles sont reecrites sur l'emplacement memoire a partir duquel elles ont ete lues en vue de leur preservation. Si les donnees sont invalides (corrompues), alors un mot de code d'echec est ecrit dans l'emplacement memoire en vue de signaler un echec de l'emplacement memoire. Le mot de code d'echec peut etre preselectionnee ou calcule dynamiquement de facon a presenter une distance mathematique superieure a tous les modeles de donnees corrigibles.

Legal Status (Type, Date, Text)
Publication 20030103 A2 Without international search report and to be republished upon receipt of that report.
Search Rpt 20031106 Late publication of international search report
Republication 20031106 A3 With international search report.

Main International Patent Class: **G06F-011/00**
Fulltext Availability:
Detailed Description

Detailed Description
... logic block 304. In various other embodiments, the failure codeword may be written into the **memory storage** device 306 via the write logic **block** 304, either with or **without** going through the **ECC** encoder 314.

The failure codeword

? t23/5,k/53-55,58,61,63

23/5,K/53 (Item 53 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00811662 **Image available**
PREPARATION OF DATA FOR A REED-SOLOMON DECODER
PREPARATION DE DONNEES DESTINEES A UN DECODEUR REED-SOLOMON
Patent Applicant/Assignee:
DEUTSCHE THOMSON-BRANDT GMBH, Hermann-Schwer-Strasse 3, 78048 Villingen-Schwenningen, DE, DE (Residence), DE (Nationality), (For all designated states except: US)
Patent Applicant/Inventor:
FREISSMANN Lothar, Beroldinger Strasse 8, 78078 Niedereschach, DE, DE (Residence), DE (Nationality), (Designated only for: US)
Legal Representative:
KURTH Dieter (agent), Deutsche Thomson-Brandt GMBH, European Patent Operations, Karl-Wiechert-Allee 74, 30625 Hannover, DE,
Patent and Priority Information (Country, Number, Date):
Patent: WO 200145271 A1 20010621 (WO 0145271)
Application: WO 2000EP12552 20001212 (PCT/WO EP0012552)
Priority Application: EP 99125014 19991215
Designated States: AE AG AL AU BA BB BG BR CA CN CR CU CZ DM DZ EE GD GE HR HU ID IL IN IS JP KP KR LC LK LR LV MA MG MK MN MX NO NZ PL RO SG SI SK TR TT UA US UZ VN YU ZA
(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR
((OAPI utility model)) BF BJ CF CG CI CM GA GN GW ML MR NE SN TD TG
(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZW
(EA) AM AZ BY KG KZ MD RU TJ TM
Main International Patent Class: H03M-013/00
International Patent Class: G11B-020/18
Publication Language: English
Filing Language: English

English Abstract
The present invention relates to a method and an arrangement for preparation of data for a Reed - Solomon decoder and more particularly to a method and an arrangement for an intelligent buffer (IBUF) in front of a ramless DVD Reed - Solomon decoder and further on particularly to a method and an arrangement for an intelligent buffer (IBUF) used also as a first pass correction **storage** of ECC- **blocks** .In such a way, the Reed - Solomon decoder will **not** get disordered **ECC blocks** by an intelligent **buffer** (IBUF) that leads to less necessary **RAM** and a high performance of the complete circuitry. The intelligent buffer (IBUF) is used as a first pass correction storage of the Reed Solomon decoder too.

French Abstract
La presente invention concerne un procede et un agencement pour la preparation de donnees destinees a un decodeur Reed-Solomon et, plus precisement, un procede et un agencement pour un tampon intelligent (IBUF) place avant un decodeur Reed-Solomon DVD sans RAM. L'invention concerne plus precisement un procede et un agencement destines a un tampon intelligent (IBUF) utilises egalement en tant qu'unite de stockage de correction a premier passage des blocs de code correcteur d'erreur (ECC). De ce fait, le decodeur Reed-Solomon ne recevra pas de bloc ECC non ordonne grace a un tampon intelligent (IBUF), necessitant ainsi moins de RAM et conduisant a une meilleure performance du circuit complet. Le tampon intelligent (IBUF) est egalement utilise en tant qu'unite de stockage de correction a premier passage du decodeur Reed-Solomon.

Legal Status (Type, Date, Text)
Publication 20010621 A1 With international search report.
Examination 20011004 Request for preliminary examination prior to end of 19th month from priority date

English Abstract
...and an arrangement for an intelligent buffer (IBUF) used also as a first pass correction **storage** of ECC- **blocks** .In such a way, the Reed - Solomon decoder will **not** get disordered **ECC blocks** by an intelligent **buffer** (IBUF) that leads to less necessary **RAM** and a high performance of the complete circuitry. The intelligent buffer (IBUF) is used as...

23/5,K/54 (Item 54 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00802534
ANY-TO-ANY COMPONENT COMPUTING SYSTEM
SYSTEME INFORMATIQUE A COMPOSANTS TOUTE CATEGORIE
Patent Applicant/Assignee:
E-BRAIN SOLUTIONS LLC, 1200 Mountain Creek Road, Suite 440, Chattanooga, TN 34705, US, US (Residence), US (Nationality), (For all designated states except: US)
Patent Applicant/Inventor:
WARREN Peter, 1200 Mountain Creek Road, Suite 440, Chattanooga, TN 37405, US, GB (Residence), GB (Nationality), (Designated only for: US)
LOWE Steven, 1625 Starboard Drive, Hixson, TN 37343, US, US (Residence), US (Nationality), (Designated only for: US)
Legal Representative:
MEHRMAN Michael J (agent), Paper Mill Village, Building 23, 600 Village Trace, Suite 300, Marietta, GA 30067, US,
Patent and Priority Information (Country, Number, Date):
Patent: WO 200135216 A2-A3 20010517 (WO 0135216)
Application: WO 2000US31231 20001113 (PCT/WO US0031231)
Priority Application: US 99164884 19991112
Designated States: AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CR CU CZ DE DK DM DZ EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG US UZ VN YU ZA ZW
(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR
(OA) BF BJ CF CG CI CM GA GN GW ML MR NE SN TD TG
(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZW
(EA) AM AZ BY KG KZ MD RU TJ TM
Main International Patent Class: G06F-009/44
International Patent Class: G06F-017/22
Publication Language: English
Filing Language: English
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 275671

English Abstract
A universal data and software structure and method for an Any-to-Any computing machine in which any number of any components can be related to any number of any other components in a manner that is not intrinsically hierarchical and is intrinsically unlimited. The structure and method includes a Concept Hierarchy; each concept or assembly of concepts is uniquely identified and assigned a number in a Numbers Concept Language

or uniquely identified in a Non-numbers Concept Language. Each Component or assembly of Components is intrinsically related to all other data items that contain common or related components.

French Abstract
L'invention concerne une structure de donnees et de logiciel universelle ainsi qu'un procede de machine informatique toute categorie dans laquelle des composants, quels qu'ils soient et quel que soit leur nombre, peuvent etre rattaches a d'autres composants, quels qu'ils soient et quel que soit leur nombre, d'une maniere intrinsequement non hierarchisee et intrinsequement illimitee. La structure et le procede comportent une hierarchie conceptuelle; chaque concept ou ensemble de concepts est identifie de maniere unique et recoit un numero dans un langage conceptuel de nombres ou dans un langage conceptuel de non-nombres. Chaque composant ou ensemble de composants est intrinsequement rattache a tous les autres elements de donnees qui contiennent des composants communs ou associes.

Legal Status (Type, Date, Text)
Publication 20010517 A2 Without international search report and to be republished upon receipt of that report.
Search Rpt 20020808 Late publication of international search report
Republication 20020808 A3 With international search report.

23/5,K/55 (Item 55 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00546701 **Image available**
MICROCONTROLLER HAVING ALLOCATION CIRCUITRY TO SELECTIVELY ALLOCATE AND/OR HIDE PORTIONS OF A PROGRAM MEMORY ADDRESS SPACE
MICROREGISSEUR COMPORTANT DES CIRCUITS D'ATTRIBUTION POUR ATTRIBUER ET/OU CACHER DE MANIERE SELECTIVE DES PARTIES D'UN ESPACE D'ADRESSE MEMOIRE DE PROGRAMME
Patent Applicant/Assignee:
SILICON STORAGE TECHNOLOGY INC,
Inventor(s):
FENG Eugene,
PHILLIPS Gary,
Patent and Priority Information (Country, Number, Date):
Patent: WO 200010074 A1 20000224 (WO 0010074)
Application: WO 99US18443 19990813 (PCT/WO US9918443)
Priority Application: US 98134242 19980814; US 98135410 19980814
Designated States: CA JP AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE
Main International Patent Class: G06F-001/24
International Patent Class: G06F-009/22
Publication Language: English
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 18028

English Abstract
A microcontroller system (104) includes program memory space allocation circuitry (104). In a first mode of operation, a first block of program memory (102a) is hidden for code fetching such that a processor is prohibited from retrieving program instructions from the first block of program memory (102a). In a second mode, however, the first block of program memory (102a) is accessible for code fetching. In a third mode of

operation, the program memory space allocation means allocates the program memory space such that the processor (103) may retrieve program instructions only from an external memory, that is not unitarily formed in the integrated circuit. In some embodiments, the mode of operation of the program memory space allocation is controlled in response to the contents of a configuration register (106). By having circuitry to so allocate the program memory, the security of the program memory (102) is enhanced.

French Abstract
L'invention concerne un systeme (104) de microregisseur comportant des circuits (104) d'attribution d'espace memoire de programme. Dans un premier mode de fonctionnement, un premier bloc de memoire (102a) de programme est cache en vue de l'extraction de codes, de sorte qu'un processeur est empeche d'extraire des instructions de programme provenant du premier bloc de memoire (102a) de programme. Dans un deuxieme mode de fonctionnement, le premier bloc de memoire (102a) de programme est accessible en vue d'une extraction de codes. Dans un troisieme mode de fonctionnement, le moyen d'attribution d'espace memoire de programme attribue l'espace memoire de programme de sorte que le processeur (103) peut extraire des instructions de programme seulement a partir d'une memoire externe, qui ne fait pas partie integrante du circuit integre. Dans certains modes de realisation, le mode de fonctionnement de l'attribution d'espace memoire de programme est commande en fonction du contenu d'un registre (106) de configuration. En faisant attribuer de cette maniere la memoire de programme par des circuits, on obtient une securite accrue de la memoire (102) de programme.

Fulltext Availability:
Claims

Claim
... is activated, the following concurTent programming operation commands are not
allowed on the locked flash **memory** **blocks** :
Sector Erase
Block Erase
Write Byte
Burst Write
Verify Byte
Entering the **Memory** **Test** Mode will **bypass** the security lock.
Therefore, besides the Chip Erase, the Enable Test and Disable Test commands...

23/5,K/58 (Item 58 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00493581 **Image available**
MERGING OF COMPRESSED RASTER IMAGES IN A PRINTING SYSTEM
FUSION DE TRAME-IMAGES COMPRIMEES DANS UN SYSTEME D'IMPRESSION
Patent Applicant/Assignee:
BARCO GRAPHICS N V,
Inventor(s):
VLIETINCK Jan J,
NOTREDAME Paul H,
DEBAERE Eddy H,
DEPUYDT Lieven W,
Patent and Priority Information (Country, Number, Date):
Patent: WO 9924933 A1 19990520

Application: WO 98BE169 19981105 (PCT/WO BE9800169)
Priority Application: US 97964651 19971105
Designated States: JP AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE
Main International Patent Class: G06K-015/02
International Patent Class: G06F-003/12
Publication Language: English
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 27051

English Abstract
This invention relates to high speed digital printing of pages each obtained by merging one or more page elements. A method is disclosed for merging page elements which are stored in a compressed format, the merging substantially in compressed domain to enable the implementation of the method to perform the merge rapidly, keeping up with a fast printing device. The merging occurs according to a page layout script which specifies the positions and printing order of selected page elements on each page. An apparatus for merging also is disclosed.

French Abstract
L'invention concerne l'impression numerique extremement rapide de pages obtenues chacune par fusion d'un ou de plusieurs elements de page. Elle concerne un procede servant a fusionner des elements de page memorises dans un format comprime, cette fusion etant realisee pratiquement sous une forme comprimee, de maniere a la rendre plus rapide afin de conserver la meme cadence qu'une imprimante rapide. Cette fusion s'effectue d'apres un schema de conception de page specifiant les positions et l'ordre d'impression d'elements de page selectionnes sur chaque page. Elle concerne egalement un dispositif de fusion.
Fulltext Availability:
Claims

Claim
... obtains the line work compressed data and the CT compressed data as required by the **page** layout script from the **page** element **cache** .

37 The system according to claim 34 wherein the compressed rasterized page element data is **unscreened** .

38 The system according to claim 34 wherein the compressed rasterized page element data is...

23/5,K/61 (Item 61 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00406196 **Image available**
DIGITAL DATA PROCESSING METHODS AND APPARATUS FOR FAULT ISOLATION
PROCEDES ET DISPOSITIF DE TRAITEMENT DE DONNEES NUMERIQUES POUR L'ISOLATION DE DEFAUTS
Patent Applicant/Assignee:
STRATUS COMPUTER,
Inventor(s):
LEAVITT William I,
CLEMSON Conrad R,
SOMERS Jeffrey S,
CHAVES John M,
BARBERA David R,

CLAYTON Shawn A,
Patent and Priority Information (Country, Number, Date):
Patent: WO 9746941 A1 19971211
Application: WO 97US9781 19970605 (PCT/WO US9709781)
Priority Application: US 96658563 19960605
Designated States: AU CA JP AT BE CH DE DK ES FI FR GB GR IE IT LU MC NL PT SE
Main International Patent Class: **G06F-011/00**
International Patent Class: G06F-11:34; G06F-11:08; G06F-11:16; G06F-11:22
Publication Language: English
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 116410

English Abstract
A fault-isolating digital data processing apparatus includes plural functional units (12-18) that are interconnected for point-to-point communications by a plurality of buses (20a-20d). The functional units (12-18) monitor the buses (20a-20d) to which they are attached and signal the other units in the event there are bus communication errors. The functional units (12-18) can simultaneously enter into an error isolation phase, e.g., in response to a bus error signalled by one of the units. In addition to signalling bus errors, the functional units can signal unit-level (or "board") faults when they detect fault in their own operation. Each unit (12 or 14) includes error isolation functionality that signals a fault based on (i) whether that unit (12 or 14) signalled a loopback error with respect to its own operation; (ii) whether that unit or another unit signalled a bus error during the error isolation phase; and/or (iii) whether any other functional unit signalled that it was faulty during the error isolation phase.

French Abstract
L'invention concerne un dispositif de traitement de donnees a isolation de defauts comprenant plusieurs unites fonctionnelles (12-18) reliees par plusieurs bus (20a-20d) pour les communications point a point. Ces unites (12-18) controlent les bus (20a-20d) auxquels elles sont reliees et s'informent reciproquement en cas d'erreurs de communications au niveau du bus. Elles (12-18) peuvent entrer simultanement dans une phase d'isolation d'erreur, par exemple suite a une erreur de bus signalee par une de ces unites. Outre la signalisation des erreurs de bus, ces unites fonctionnelles indiquent les defauts l'echelon de l'unite (ou de la "carte") si elles decelent un defaut dans leur fonctionnement propre. On prevoit chaque unite (12 ou 14) des fonctions d'isolation d'erreur signalant un defaut selon les criteres suivants: (i) l'unite a indique une erreur de signal de retour liee a son fonctionnement propre; (ii) l'unite consideree ou une autre unite a signale une erreur de bus pendant la phase d'isolation d'erreur; et/ou (iii) toute autre unite fonctionnelle a signale que son propre fonctionnement etait defectueux durant la phase d'isolation d'erreur.

Main International Patent Class: **G06F-011/00**
Fulltext Availability:
Detailed Description

Detailed Description
... in PCI memory space impacts the fault tolerance. In order to keep the 4-4K **pages** that make up the 16K **page** contguous in PCI **memory** space, the 2 **pages** bits of the IOVA bits 11 3:12) are **not checked** under the checksum. In the case of an error this could allow a controller to...

23/5,K/63 (Item 63 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00271568 **Image available**

INTERMEDIATE PROCESSOR DISPOSED BETWEEN A HOST PROCESSOR CHANNEL AND A STORAGE DIRECTOR WITH ERROR MANAGEMENT

PROCESSEUR INTERMEDIAIRE PLACE ENTRE UN CANAL DE PROCESSEUR D'ORDINATEUR CENTRAL ET UN PROCESSEUR DE MEMORISATION A GESTION D'ERREUR

Patent Applicant/Assignee:
ANDOR SYSTEMS INC,
Inventor(s):
BERGSTEN James R,
HWANG Shih-Tsung,
KING David J,

Patent and Priority Information (Country, Number, Date):
Patent: WO 9419743 A1 19940901
Application: WO 94US1447 19940209 (PCT/WO US9401447)
Priority Application: US 9318635 19930217
Designated States: JP AT BE CH DE DK ES FR GB GR IE IT LU MC NL PT SE
Main International Patent Class: **G06F-011/00**
Publication Language: English
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 8948

English Abstract

An intermediate processor (22) includes a main processor coupled to a plurality of front end circuits, and each front end circuit is coupled to a plurality of control unit interface circuits. Each control unit interface circuit is coupled to host computers (21, 22, 23) through channels (24-29). Any control unit interface circuit may communicate with any front end circuit. The main processor is also coupled to a plurality of mass storage devices (64, 66, 68) through a plurality of channel of back end circuits. Tracks of data from the mass storage devices are stored in a main storage memory located in the main processor. A unique buffer circuit allows data to be communicated between the main processor and the circuits coupled to it immediately without requiring the circuits to operate at the main processor clocking rate. Each front end circuit includes a nonvolatile storage memory for storing change data sufficinet to update the mass storage devices in the event of a power or hardware failure.

French Abstract

Un processeur intermediaire (22) comprend un processeur principal couple a une pluralite de circuits terminaux avant, chaque circuit terminal avant etant couple a une pluralite de circuits d'interfaces d'unite de commande. Chaque circuit d'interface d'unite de commande est couple a des ordinateurs centraux (21, 22, 23) par l'intermediaire de canaux (24-29). N'importe quel circuit d'interface d'unites de commande peut communiquer avec n'importe quel circuit terminal avant. Le processeur principal est egalement couple a une pluralite de memoires de grande capacite (64, 66, 68) par l'intermediaire d'une pluralite de canaux ou circuits terminaux arriere. Des pistes de donnees provenant des memoires de grande capacite sont stockees dans une memoire principale situee dans le processeur principal. Un circuit de tampons unique permet de communiquer immediatement les donnees entre le processeur principal et les circuits complets a celui-ci sans exiger que les circuits fonctionnent au commencement du processeur principal. Chaque circuit terminal avant

comprend une memoire remanente pour stocker des donnees de modification suffisante afin de mettre a jour les memoires de grande capacite en cas de panne de courant ou de defaillance du materiel.

Main International Patent Class: **G06F-011/00**
Fulltext Availability:
Detailed Description

Detailed Description
... CH circuit 90A-H accepts CCW chains created by main processor 74 and executes them (**without checking** for validity or correct length) using the OEMI bus and tag protocol. The CH circuits also accept status information and **, blocks** of data from the **storage** directors for main processor 7 4 e Each CH circuit can read and write directly...
?

```
File 696:DIALOG Telecom. Newsletters 1995-2004/Jan 07
         (c) 2004 The Dialog Corp.
File  15:ABI/Inform(R) 1971-2004/Jan 08
         (c) 2004 ProQuest Info&Learning
File 484:Periodical Abs Plustext 1986-2004/Jan W1
         (c) 2004 ProQuest
File 813:PR Newswire 1987-1999/Apr 30
         (c) 1999 PR Newswire Association Inc
File 635:Business Dateline(R) 1985-2004/Jan 08
         (c) 2004 ProQuest Info&Learning
File 810:Business Wire 1986-1999/Feb 28
         (c) 1999 Business Wire
File 369:New Scientist 1994-2003/Dec W2
         (c) 2003 Reed Business Information Ltd.
File 370:Science 1996-1999/Jul W3
         (c) 1999 AAAS
File  20:Dialog Global Reporter 1997-2004/Jan 08
         (c) 2004 The Dialog Corp.
File 624:McGraw-Hill Publications 1985-2004/Jan 07
         (c) 2004 McGraw-Hill Co. Inc
File 634:San Jose Mercury  Jun 1985-2003/Dec 31
         (c) 2004 San Jose Mercury News
File 647:CMP  Computer Fulltext 1988-2004/Dec W4
         (c) 2004 CMP Media, LLC
File 674:Computer News Fulltext 1989-2003/Dec W3
         (c) 2003 IDG Communications
? ds

Set     Items   Description
S1    1845058   PAGE OR PAGES
S2     899385   BLOCK? ?
S3    1484239   STORAGE OR MEMORY OR BUFFER? ? OR CACHE? ? OR RAM OR ROM OR
               PROM OR EPROM OR FPROM OR CDROM? ?
S4      13056   EDAC OR ECC OR HAMMING
S5      32221   DEBUG? OR DE()BUG???? ?
S6   11925460   CHECK??? ? OR DETECT??? ? OR DIAGNOS???? ? OR DX OR ANALYZ?
               OR ANALYS? OR ANALYT? OR LOOK??? ? OR EXAMIN? OR SCREEN?
S7    8809956   SCRUTIN? OR REVIEW? OR EVALUAT? OR INSPECT? OR MONITOR? OR
              TEST OR TESTS OR TESTED OR TESTING OR SCAN OR SCANS OR SCANNED
               OR SCANNING
S8     297032   ('NOT' OR WITHOUT)(1W)S6:S7
S9      52888   UNCHECK? OR UNEXAMIN? OR UNSCREEN? OR UNSCRUTIN? OR UNREVI-
              EW? OR UNEVALUAT? OR UNINSPECT? OR UNMONITOR? OR UNSCAN????? ?
               OR UNTEST??? ?
S10      1342   S4:S5(3N)('NOT' OR WITHOUT)
S11   2951603   BYPASS? OR BY()PASS??? ? OR AVOID? OR SKIP???? ? OR IGNOR?
              OR DISREGARD? OR EXCLUD? OR EXCLUSION? OR PASS???()OVER
S12         0   'BY'()PASS??? ?
S13     70761   S11:S12(3N)S4:S7
S14     14002   S1:S2(5N)S3
S15        53   S14(S)(S8:S10 OR S13)
S16        27   S15/1999:2004
S17        26   S15 NOT S16
S18        22   RD (unique items)
? t18/3,k/21,22

 18/3,K/21     (Item 3 from file: 647)
DIALOG(R)File 647:CMP  Computer Fulltext
(c) 2004 CMP Media, LLC. All rts. reserv.
```

00549551 CMP ACCESSION NUMBER: WIN19930401S7916
Optimizing Windows - Squeeze All the Memory You Can From Your PC
Brian Livingston
WINDOWS MAGAZINE, 1993, n 404 , 307
PUBLICATION DATE: 930401
JOURNAL CODE: WIN LANGUAGE: English
RECORD TYPE: Fulltext
SECTION HEADING: HOW TO
WORD COUNT: 2956

... following command:
WIN /D:X
The switch /D:X places Windows in a so-called **debugging** mode and **excludes** all upper **memory blocks** from Windows' use. In this situation, Windows is forced to locate its translation buffers into...

18/3,K/22 (Item 1 from file: 674)
DIALOG(R)File 674:Computer News Fulltext

070105
Enterprise caching: Smart or smoke?
Byline: Thomas Nolle
Journal: Network World Page Number: 47
Publication Date: November 09, 1998
Word Count: 809 Line Count: 69

Text:
... faster and reduces traffic on the Internet. However, caching is limited. With browser caches, the **cache** stores one user's **pages** and is accessible only to that user. If the user at the next desk loads...

... server, at a place where many users would pass through to access Web content. The **cache** server stores **pages** accessed by any of the users whose requests and responses pass through them.Caching can...

...for billing, a cache will defeat the process by intercepting the request and filling it **without** security **checks** or counting. The final issue with caching is cost. Let's suppose you have an...
?

```
File   2:INSPEC 1969-2003/Dec W2
         (c) 2003 Institution of Electrical Engineers
File   6:NTIS 1964-2004/Jan W1
         (c) 2004 NTIS, Intl Cpyrght All Rights Res
File   8:Ei Compendex(R) 1970-2004/Dec W4
         (c) 2004 Elsevier Eng.  Info. Inc.
File  34:SciSearch(R) Cited Ref Sci 1990-2003/Dec W4
         (c) 2003 Inst for Sci Info
File  35:Dissertation Abs Online 1861-2003/Nov
         (c) 2003 ProQuest Info&Learning
File  65:Inside Conferences 1993-2004/Jan W1
         (c) 2004 BLDSC all rts. reserv.
File  94:JICST-EPlus 1985-2004/Dec W4
         (c)2004 Japan Science and Tech Corp(JST)
File  95:TEME-Technology & Management 1989-2004/Dec W3
         (c) 2004 FIZ TECHNIK
File  99:Wilson Appl. Sci & Tech Abs 1983-2003/Nov
         (c) 2003 The HW Wilson Co.
File 111:TGG Natl.Newspaper Index(SM) 1979-2004/Jan 06
         (c) 2004 The Gale Group
File 144:Pascal 1973-2003/Dec W2
         (c) 2003 INIST/CNRS
File 202:Info. Sci. & Tech. Abs. 1966-2003/Nov 17
         (c) 2003 EBSCO Publishing
File 233:Internet & Personal Comp. Abs. 1981-2003/Sep
         (c) 2003 EBSCO Pub.
File 266:FEDRIP 2003/Nov
         Comp & dist by NTIS, Intl Copyright All Rights Res
File 434:SciSearch(R) Cited Ref Sci 1974-1989/Dec
         (c) 1998 Inst for Sci Info
File 483:Newspaper Abs Daily 1986-2004/Jan 07
         (c) 2004 ProQuest Info&Learning
File 603:Newspaper Abstracts 1984-1988
         (c)2001 ProQuest Info&Learning
? ds

Set     Items   Description
S1     464788   PAGE OR PAGES
S2     663432   BLOCK? ?
S3    1771411   STORAGE OR MEMORY OR BUFFER? ? OR CACHE? ? OR RAM OR ROM OR
               PROM OR EPROM OR FPROM OR CDROM? ?
S4      16484   EDAC OR ECC OR HAMMING
S5      37383   DEBUG? OR DE()BUG???? ?
S6   18436435   CHECK??? ? OR DETECT??? ? OR DIAGNOS???? ? OR DX OR ANALYZ?
               OR ANALYS? OR ANALYT? OR LOOK??? ? OR EXAMIN? OR SCREEN?
S7   13172909   SCRUTIN? OR REVIEW? OR EVALUAT? OR INSPECT? OR MONITOR? OR
               TEST OR TESTS OR TESTED OR TESTING OR SCAN OR SCANS OR SCANNED
               OR SCANNING
S8     129534   ('NOT' OR WITHOUT)(1W)S6:S7
S9      11842   UNCHECK? OR UNEXAMIN? OR UNSCREEN? OR UNSCRUTIN? OR UNREVI-
               EW? OR UNEVALUAT? OR UNINSPECT? OR UNMONITOR? OR UNSCAN????? ?
               OR UNTEST??? ?
S10       942   S4:S5(3N)('NOT' OR WITHOUT)
S11   1118147   BYPASS? OR BY()PASS??? ? OR AVOID? OR SKIP???? ? OR IGNOR?
               OR DISREGARD? OR EXCLUD? OR EXCLUSION? OR PASS???()OVER
S12         0   'BY'()PASS??? ?
S13     58255   S11:S12(3N)S4:S7
S14     11763   S1:S2(5N)S3
S15        65   S14 AND (S8:S10 OR S13)
S16        27   S15/1999:2003
S17        38   S15 NOT S16
```

S18 30 RD (unique items)
? t18/7/1,12-13

18/7/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

5769176 INSPEC Abstract Number: A9802-9510C-001, C9801-7350-021
Title: A parallel tree code for large N-body simulation: dynamic load balance and data distribution on a CRAY T3D system
Author(s): Becciani, U.; Ansaloni, R.; Antonuccio-Delogu, V.; Erbacci, G. ; Gambera, M.; Pagliaro, A.
Author Affiliation: Osservatorio Astrofisico di Catania, Citta Univ., Catania, Italy
Journal: Computer Physics Communications vol.106, no.1-2 p.105-13
Publisher: Elsevier,
Publication Date: Oct. 1997 Country of Publication: Netherlands
CODEN: CPHCBZ ISSN: 0010-4655
SICI: 0010-4655(199710)106:1/2L.105:PTCL;1-7
Material Identity Number: C083-97012
U.S. Copyright Clearance Center Code: 0010-4655/97/$17.00
Document Number: S0010-4655(97)00102-1
Language: English Document Type: Journal Paper (JP)
Treatment: Theoretical (T)
Abstract: N-body algorithms for long-range **unscreened** interactions like gravity belong to a class of highly irregular problems whose optimal solution is a challenging task for present-day massively parallel computers. In this paper we describe a strategy for optimal memory and work distribution which we have applied to our parallel implementation of the Barnes & Hut (1986) recursive tree scheme on a Cray T3D using the CRAFT programming environment. We have performed a series of tests to find an optimal data distribution in the T3D memory, and to identify a strategy for the Dynamic Load Balance in order to obtain good performances when running large simulations (more than 10 million particles). The results of tests show that the step duration depends on two main factors: the data locality and the T3D network contention. Increasing data locality we are able to minimize the step duration if the closest bodies (direct interaction) tend to be located in the same PE local **memory** (contiguous **block** subdivision, high granularity), whereas the tree properties have a fine grain distribution. In a very large simulation, due to network contention, an unbalanced load arises. To remedy this we have devised an automatic work redistribution mechanism which provided a good Dynamic Load Balance at the price of an insignificant overhead. (14 Refs)
Subfile: A C

18/7/12 (Item 12 from file: 2)
DIALOG(R)File 2:INSPEC

02050379 INSPEC Abstract Number: B83031528
Title: Basic investigations on a dual-color picture-display panel using two-dimensional array of light-emitting diodes
Author(s): Fujii, T.; Fujita, A.
Author Affiliation: Faculty of Engng., Shiznoka Univ., Hamamatsu, Japan
Journal: Reports of the Faculty of Engineering, Shizuoka University no.32 p.61-77
Publication Date: 1981 Country of Publication: Japan
CODEN: SDKKAT ISSN: 0583-0915
Language: Japanese Document Type: Journal Paper (JP)

ISSN: 0888-8507
Company Name: Quarterdeck Office Systems
Product Name: QEMM-386

Presents a very favorable review of QEMM-386 version 6.0 ($99.95), a memory manager from Quarterdeck Office Systems Inc., Santa Monica, CA (213). The program requires a 386- or 486-based system with DOS 3.0 or later. The program copies ROM to extended memory and uses the **ROM** address space for Upper **Memory Block memory** . This requires that the **ROM** code must not contain hard-coded addresses and access to it must be through system interrupts that QEMM can monitor. Using the program on a typical system will result in a gain of 83K of UMB memory, but PS/2 users can gain more than 140K. In benchmark testing, using QEMM resulted in a 40 percent increase in time required for the video BIOS write **without** scroll **test** , but since calls to this BIOS are infrequent the memory gain compensates for the speed decrease. (djd)

?

File 256:SoftBase:Reviews,Companies&Prods. 82-2004/Dec
(c)2004 Info.Sources Inc
? ds

Set	Items	Description
S1	8401	PAGE OR PAGES
S2	1856	BLOCK? ?
S3	12188	STORAGE OR MEMORY OR BUFFER? ? OR CACHE? ? OR RAM OR ROM OR PROM OR EPROM OR FPROM OR CDROM? ?
S4	21	EDAC OR ECC OR HAMMING
S5	1456	DEBUG? OR DE()BUG???? ?
S6	3229	BYPASS? OR BY()PASS??? ? OR AVOID? OR SKIP???? ? OR IGNOR? OR DISREGARD? OR EXCLUD? OR EXCLUSION? OR PASS???()OVER
S7	166	('NOT' OR WITHOUT)(1W)(CHECK??? ? OR DIAGNOS???? ? OR DX OR ANALYZ? OR ANALYS? OR ANALYT? OR LOOK??? ? OR EXAMIN? OR SCREEN?)
S8	32291	CHECK??? ? OR DIAGNOS???? ? OR DX OR ANALYZ? OR ANALYS? OR ANALYT? OR LOOK??? ? OR EXAMIN? OR SCREEN?
S9	27156	SCRUTIN? OR REVIEW? OR EVALUAT? OR INSPECT? OR MONITOR? OR TEST OR TESTS OR TESTED OR TESTING OR SCAN OR SCANS OR SCANNED OR SCANNING
S10	78	UNCHECK? OR UNEXAMIN? OR UNSCREEN? OR UNSCRUTIN? OR UNREVIEW? OR UNEVALUAT? OR UNINSPECT? OR UNMONITOR? OR UNSCAN????? ? OR UNTEST??? ?
S11	202	('NOT' OR WITHOUT)(1W)S9
S12	119	S6(3N)S8:S9
S13	192	S1:S2(5N)S3
S14	43	(S6 OR 'NOT' OR WITHOUT)(3N)S4:S5
S15	1	S13 AND (S14 OR S7 OR S10:S12)

? t15/k

15/K/1
DIALOG(R)File 256:(c)2004 Info.Sources Inc. All rts. reserv.

...search sites. Although the two products seem unrelated, there is a correlation. Search engines do **not** actually **examine** the Web directly, but an index of the Web. The engine uses search algorithms to...

...works in a similar way, storing pages located downstream that are frequently requested by users. **Cached pages** can also be reduced in the same way Web pages are reduced to an index...
?

File 347:JAPIO Oct 1976-2003/Sep(Updated 040105)
(c) 2004 JPO & JAPIO
File 350:Derwent WPIX 1963-2004/UD,UM &UP=200402
(c) 2004 Thomson Derwent
? ds

Set	Items	Description
S1	71131	PAGE OR PAGES
S2	928570	BLOCK? ?
S3	1823159	STORAGE OR MEMORY OR BUFFER? ? OR CACHE? ? OR RAM OR ROM OR PROM OR EPROM OR FPROM OR CDROM? ?
S4	2925	EDAC OR ECC OR HAMMING
S5	8843	DEBUG? OR DE()BUG???? ?
S6	2690193	CHECK??? ? OR DETECT??? ? OR DIAGNOS???? ? OR DX OR ANALYZ? OR ANALYS? OR ANALYT? OR LOOK??? ? OR EXAMIN? OR SCREEN?
S7	1476916	SCRUTIN? OR REVIEW? OR EVALUAT? OR INSPECT? OR MONITOR? OR TEST OR TESTS OR TESTED OR TESTING OR SCAN OR SCANS OR SCANNED OR SCANNING
S8	28467	('NOT' OR WITHOUT)(1W)S6:S7
S9	898	UNCHECK? OR UNEXAMIN? OR UNSCREEN? OR UNSCRUTIN? OR UNREVIEW? OR UNEVALUAT? OR UNINSPECT? OR UNMONITOR? OR UNSCAN????? ? OR UNTEST??? ?
S10	646	S4:S5(3N)('NOT' OR WITHOUT)
S11	672734	BYPASS? OR BY()PASS??? ? OR AVOID? OR SKIP???? ? OR IGNOR? OR DISREGARD? OR EXCLUD? OR EXCLUSION? OR PASS???()OVER
S12	70120	'BY'()PASS??? ?
S13	14910	S11:S12(3N)S4:S7
S14	41141	S1:S2(5N)S3
S15	222	S14 AND (S8:S10 OR S13)
S16	29667	IC='H04L-009'
S17	85758	IC='G06F-011'
S18	1554	MC='T01-G01A'
S19	32	S15 AND S16:S18
S20	32	IDPAT (sorted in duplicate/non-duplicate order)
S21	32	IDPAT (primary/non-duplicate records only)

? t21/9/10-11,14,17-18

21/9/10 (Item 10 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2004 Thomson Derwent. All rts. reserv.

013536178 **Image available**
WPI Acc No: 2001-020384/200103
XRPX Acc No: N01-015654

Large scale memory management procedure in information processor, involves checking minimum required memory area of memory, when operating system is started

Patent Assignee: MITSUBISHI ELECTRIC CORP (MITQ)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 2000293391	A	20001020	JP 99100538	A	19990407	200103	B

Priority Applications (No Type Date): JP 99100538 A 19990407
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 2000293391	A		26	G06F-011/20	

Abstract (Basic): JP 2000293391 A
NOVELTY - The minimum required memory area in memory is checked, when operating system is started. The memory area in memory which is

not checked , when operating system is started, is not used.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for large scale memory management system.

USE - For managing large scale memory in information processor such as computer system.

ADVANTAGE - The starting time of operating system is reduced.

DESCRIPTION OF DRAWING(S) - The figure shows the **block** diagram of large scale **memory** management system.

pp; 26 DwgNo 1/14

Title Terms: SCALE; MEMORY; MANAGEMENT; PROCEDURE; INFORMATION; PROCESSOR; CHECK; MINIMUM; REQUIRE; MEMORY; AREA; MEMORY; OPERATE; SYSTEM; START

Derwent Class: T01; U21

International Patent Class (Main): **G06F-011/20**

International Patent Class (Additional): G06F-009/06; G06F-012/00; G06F-012/16

File Segment: EPI

Manual Codes (EPI/S-X): T01-F06; T01-G03; T01-H; T01-H01C4; U21-A06

21/9/11 (Item 11 from file: 350)

DIALOG(R)File 350:Derwent WPIX

013199541 **Image available**

WPI Acc No: 2000-371414/200032

XRPX Acc No: N00-278439

Sharing memory management system for exclusion control of disk drive, has program modules to control usage of sharing memory storing exclusion management information

Patent Assignee: PFU KK (USAE)

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 2000122885	A	20000428	JP 98293985	A	19981015	200032	B

Priority Applications (No Type Date): JP 98293985 A 19981015

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 2000122885	A		7	G06F-011/22	

Abstract (Basic): JP 2000122885 A

NOVELTY - A table in a sharing memory (2), stores information for **exclusion** management of **testing** apparatus (3). Approval or rejection of usage rights of sharing memory is performed by release module (103) of diagnostic programs (1A,1B). Information for performing **exclusion** management of **testing** apparatus is deleted or registered by control modules (104,105).

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for recording medium for storing sharing memory management system.

USE - For exclusion control of partial area of disk drive, memory device, etc.

ADVANTAGE - **Exclusion** management control of **testing** apparatus is performed at high speed, as sharing memory is used. As exclusion control of partial area of testing apparatus is done, testing load is reduced and testing efficiency is increased remarkably.

DESCRIPTION OF DRAWING(S) - The figure shows the component **block** diagram of sharing **memory** management system.

Diagnostic program (1A,1B)

Memory (2)

Testing apparatus (3)

Release module (103)
Control modules (104,105)
pp; 7 DwgNo 1/8
Title Terms: SHARE; MEMORY; MANAGEMENT; SYSTEM; EXCLUDE; CONTROL; DISC; DRIVE; PROGRAM; MODULE; CONTROL; SHARE; MEMORY; STORAGE; EXCLUDE; MANAGEMENT; INFORMATION
Derwent Class: T01
International Patent Class (Main): **G06F-011/22**
International Patent Class (Additional): G06F-012/00
File Segment: EPI
Manual Codes (EPI/S-X): T01-F05E; T01-H01B1; T01-S03

21/9/14 (Item 14 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012360866 **Image available**
WPI Acc No: 1999-166973/199914
XRPX Acc No: N99-121685
Data blocks backing-up and restoring method for database system
Patent Assignee: ORACLE CORP (ORAC-N)
Inventor: KLEIN J D
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5873101	A	19990216	US 97799562	A	19970210	199914	B

Priority Applications (No Type Date): US 97799562 A 19970210
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5873101	A		12	G06F-011/00	

Abstract (Basic): US 5873101 A
NOVELTY - Data blocks (215) are copied from a database to a storage medium (250), **without analyzing** their contents based on initial configuration. The data **blocks** are then copied from **storage** medium to database, according to a final configuration. Any location based information reflecting initial configuration is identified and updated by analyzing block contents, according to final configuration, by mutual map comparison.
DETAILED DESCRIPTION - INDEPENDENT CLAIMS are included for the following:
(a) a computer readable medium;
(b) a computer system.
USE - For back-up or restore and bulk data transfer in database system.
ADVANTAGE - Provides flexibility of logical back-up and favorable performance characteristics of physical back-up.
DESCRIPTION OF DRAWING(S) - The figure is a block diagram illustrating back-up of data.
Data blocks (215)
Storage medium (250)
pp; 12 DwgNo 2/4
Title Terms: DATA; BLOCK; BACKING; UP; RESTORATION; METHOD; DATABASE; SYSTEM
Derwent Class: T01
International Patent Class (Main): **G06F-011/00**
File Segment: EPI
Manual Codes (EPI/S-X): T01-F05E; T01-G03; T01-J05B2; T01-J05B4P

21/9/17 (Item 17 from file: 350)
DIALOG(R)File 350:Derwent WPIX

009916012 **Image available**
WPI Acc No: 1994-183722/199422
XRPX Acc No: N94-145017

Data storage system having stale data detector - includes user data store having addressable user data storage locations and flag data store

Patent Assignee: AMPEX CORP (AMPE); AMPEX SYSTEMS CORP (AMPE)
Inventor: BERTRAND K J
Number of Countries: 019 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 9411800	A2	19940526	WO 93US11072	A	19931115	199422	B
US 5438575	A	19950801	US 92976870	A	19921116	199536	

Priority Applications (No Type Date): US 92976870 A 19921116
Cited Patents: No-SR.Pub
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 9411800	A2	E	26	G06F-000/00	
	Designated States (National): GB JP KR				
	Designated States (Regional): AT BE CH DE DK ES FR GB GR IE IT LU MC NL PT SE				
US 5438575	A		12	G06F-011/00	

Abstract (Basic): WO 9411800 A

The data storage system includes a user data store which has a number of addressable user data storage locations coupled to store and retrieve data in response to received addresses. A flag data store is provided which has addressable flag data storage locations. Each flag data storage location corresponds to an addressable user data storage location, and has two stale data flag bits.

The system further includes a control circuit which is coupled to the addressable flag data store and assigns the two flag bits to different alternate blocks of received data. When reading, the corresponding assigned flag bit is output as a stale or invalid data signal and the non-assigned flag bit is set to a second state different from the first state in preparation for the next block of data.

ADVANTAGE - High speed and low cost.

Dwg.1/5

Abstract (Equivalent): US 5438575 A

The data storage system has two flag data storage bits provided for each word location in addition to the normal data **storage** bits. As **blocks** of data are received by the storage system one of the two flag bits is assigned to the block on an alternating basis.

Upon writing data to an address location, an assigned flab bit is written to a first state to indicate valid data. When reading, the corresponding assigned flag bit is output as a stale or invalid data signal and the non-assigned flat bit is set to a second state different from the first state in preparation for the next block of data.

USE/ADVANTAGE - Low cost, high speed data storage system provides word-by-word stale data **detection** while **avoiding** need to both read and write single memory location during memory read operation.

Dwg.1/5

Title Terms: DATA; STORAGE; SYSTEM; STALE; DATA; DETECT; USER; DATA; STORAGE; ADDRESS; USER; DATA; STORAGE; LOCATE; FLAG; DATA; STORAGE
Derwent Class: T01
International Patent Class (Main): **G06F-011/00**

International Patent Class (Additional): G08C-025/00; H03M-013/00;
H04L-001/00
File Segment: EPI
Manual Codes (EPI/S-X): T01-G01

21/9/18 (Item 18 from file: 350)
DIALOG(R)File 350:Derwent WPIX

009332873
WPI Acc No: 1993-026336/199303
XRPX Acc No: N93-020092
Cache memory without **validity** check **bit - uses special address written to address tag space of cache register to indicate validity, pref. from** memory block **only used at start-up, so all main memory can be cached**
Patent Assignee: ANONYMOUS (ANON)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
TP 129203	A	19921225	TP 92129203	A	19921220	199303	B

Priority Applications (No Type Date): TP 92129203 A 19921220
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
TP 129203	A		1	G06F-000/00	

Abstract (Basic): TP 129203 A
The cache memory does not have an extra validity bit. To indicate validity a special address written to the address tag space of a cache register indicates validity, e.g. FFFF. If this address is in the address space, the data is invalid. If any other address is used, the data is valid.
A potential disadvantage is that data from main **memory** in the **block** represented by the ''invalid'' address cannot be cached. In a preferred embodiment, to avoid this, the address used to denote invalidity is from a **block** of **memory** only used at start up and never addressed after, such as the Top-BIOS **block** in high **memory** .
USE/ADVANTAGE - Cache memory implemented without need for ''extra'' bit to denote validity.
Dwg.0/0
Title Terms: CACHE; MEMORY; VALID; CHECK; BIT; SPECIAL; ADDRESS; WRITING; ADDRESS; TAG; SPACE; CACHE; REGISTER; INDICATE; VALID; PREFER; MEMORY; BLOCK; START; UP; SO; MAIN; MEMORY; CAN
Derwent Class: T01
International Patent Class (Main): G06F-000/00
File Segment: EPI
Manual Codes (EPI/S-X): T01-F05B; **T01-G01A** ; T01-H03A
? t21/9/25,27-28

21/9/25 (Item 25 from file: 347)
DIALOG(R)File 347:JAPIO

04048953 **Image available**
DEBUGGING DEVICE AND METHOD

PUB. NO.: 05-040653 [JP 5040653 A]
PUBLISHED: February 19, 1993 (19930219)

INVENTOR(s): ISHIKAWA TSUTOMU
ASAI OSAMU
OTA TAKANORI
SATO HIDEKI
YOSHIZAWA RYOKICHI
APPLICANT(s): HITACHI LTD [000510] (A Japanese Company or Corporation), JP (Japan)
HITACHI PROCESS COMPUT ENG INC [485525] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 03-197728 [JP 91197728]
FILED: August 07, 1991 (19910807)
INTL CLASS: [5] **G06F-011/28** ; G06F-012/10
JAPIO CLASS: 45.1 (INFORMATION PROCESSING -- Arithmetic Sequence Units); 45.2 (INFORMATION PROCESSING -- Memory Units)
JOURNAL: Section: P, Section No. 1562, Vol. 17, No. 332, Pg. 157, June 23, 1993 (19930623)

ABSTRACT

PURPOSE: To enable a **debugging** operation **without** affecting the execution of a non-debug program by operating a virtual-real address table and assigning the common resources to a unique real memory for each program.

CONSTITUTION: When a common program is debugged, a debugger 103 requests the common program to set a break point. In the break point setting process 104, a real **memory** 707 and a **page** table 708 are secured with the processing 702 where a designated address is decided. Then the address of the memory 707 secured for a program to be debugged is set at a **page** entry 709. Furthermore the **memory** contents 712 of a **page** including a break point inserting address are copied to the memory 707 in a real memory 710 prepared for a non-debug program. Thus a break point is set to the memory 707 only.

21/9/27 (Item 27 from file: 347)
DIALOG(R)File 347:JAPIO

02379339 **Image available**
ERROR PROCESSING SYSTEM

PUB. NO.: 62-296239 [JP 62296239 A]
PUBLISHED: December 23, 1987 (19871223)
INVENTOR(s): OSONE HIDEKI
TANAKA TSUTOMU
APPLICANT(s): FUJITSU LTD [000522] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 61-139727 [JP 86139727]
FILED: June 16, 1986 (19860616)
INTL CLASS: [4] **G06F-011/00** ; **G06F-011/34**
JAPIO CLASS: 45.1 (INFORMATION PROCESSING -- Arithmetic Sequence Units)
JOURNAL: Section: P, Section No. 711, Vol. 12, No. 188, Pg. 163, June 02, 1988 (19880602)

ABSTRACT

PURPOSE: To facilitate the retrial of an IPL by generating an error and separating an error generating block when the error occurs when a machine checking mask is off.
CONSTITUTION: When a machine checking mask is off, a signal bypass circuit 10 is operated, an error counter 4 is **bypassed** , an error **checking** signal is sent to a deleting register 5 and the **block** including the **RAM**

of the error generation can be separated. Thus, even when the machine checking mask is off, the defective block can be separated by a first block error, and even when a first IPL (INITIAL PROCRAM LOAD) is not successful, the second IPL can be executed.

21/9/28 (Item 28 from file: 347)
DIALOG(R)File 347:JAPIO

01868146 **Image available**
SELF-DIAGNOSIS CONTROLLING SYSTEM IN CASE OF RISE OF SYSTEM

PUB. NO.: 61-082246 [JP 61082246 A]
PUBLISHED: April 25, 1986 (19860425)
INVENTOR(s): TSURU MASAFUMI
APPLICANT(s): TOSHIBA CORP [000307] (A Japanese Company or Corporation), JP (Japan)
TOSHIBA COMPUT ENG CORP [486760] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 59-204255 [JP 84204255]
FILED: September 29, 1984 (19840929)
INTL CLASS: [4] **G06F-011/22** ; G06F-001/00; G06F-012/16
JAPIO CLASS: 45.1 (INFORMATION PROCESSING -- Arithmetic Sequence Units); 45.2 (INFORMATION PROCESSING -- Memory Units); 45.9 (INFORMATION PROCESSING -- Other)
JAPIO KEYWORD: R129 (ELECTRONIC MATERIALS -- Super High Density Integrated Circuits, LSI & GS; R131 (INFORMATION PROCESSING -- Microcomputers & Microprocessers)
JOURNAL: Section: P, Section No. 493, Vol. 10, No. 256, Pg. 23, September 02, 1986 (19860902)

ABSTRACT

PURPOSE: To shorten a system rise time by checking whether a memory **test skip** instruction exists or not, in a memory test period, discontinuing its memory test, when it has become significant, and shifting the processing to an IPL.

CONSTITUTION: When a power source of a system is turned on, an operating test of a principal LSI and its initializing are executed, and if it is normal, a memory test is executed. When executing the **memory** test, 16k bytes are one **block** , data is written (Write) to an effective memory size, its data is read out (Read), and this Read/Write data is compared. In this case, a key input for detecting a memory error and a memory **test skip** is **checked** at every 16k bytes. When checking the key input,, an interruption, etc. are used, whether the key input exists or **not** is **checked** by reading the contents of a specified flag (register area 23), and when the key input is detected, the memory test is discontinued, and the processing is shifted to an IPL.

US 094592870EP1

Creation date: 12-13-2004
Indexing Officer: STANOH - SIMON TANOH
Team: OIPEBackFileIndexing
Dossier: 09459287

Legal Date: 01-15-2004

No.	Doccode	Number of pages
1	CTFR	9
2	892	1
3	NPL	6
4	NPL	6

Total number of pages: 22

Remarks:

Order of re-scan issued on .....